

Compal Confidential

KALG1- M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

2009-04-17

REV 01

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File Name : LA-XXXXP

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75VS power rail for DDR3 terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for NB(LVDS)	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3V	3.3V power rail for SB	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail for SB	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 100X b

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS367, SLG8SP556V)	1101 001Xb
DDR2 DIMMA	1001 000Xb
DDR2 DIMMB	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1				
2				
3				
4				
5				
6				
7				

BOARD ID Table

Board ID	PCB Revision
0	PCB 08Y LA-5271P REV1 M/B
1	
2	
3	
4	
5	
6	
7	



BTO Option Table

BTO Item	BOM Structure
GL40	GL40@
GM45	GM45@

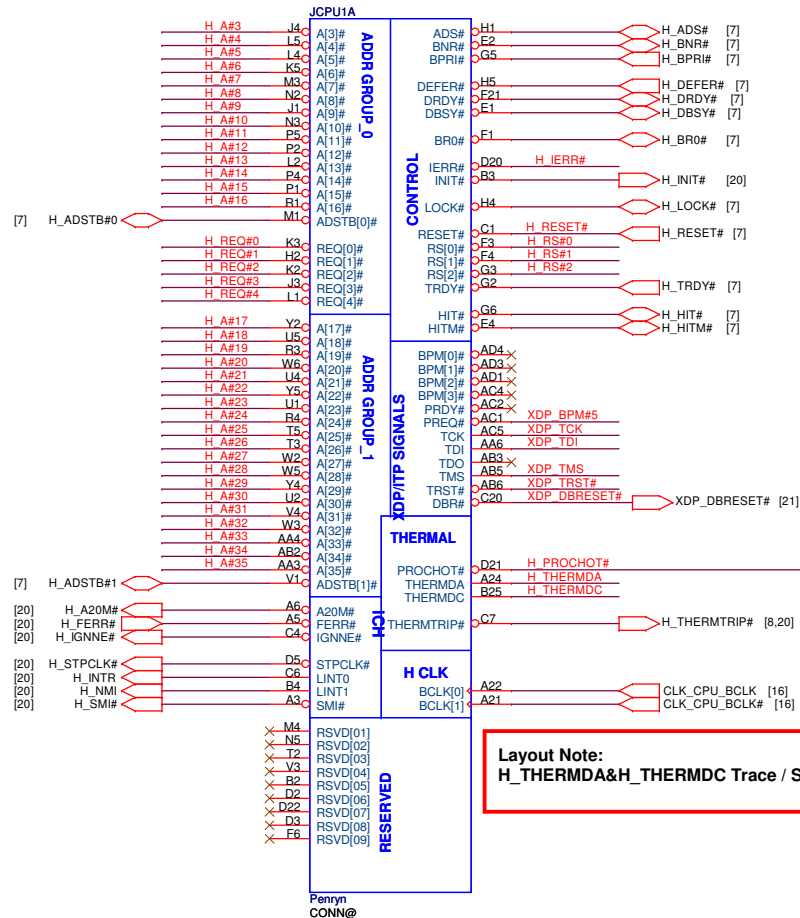
BOM Configuration Table

Project	BOM Configuration
KALG1_GM45	GM45@/KALG1@/KAL90_G0_90+@
KALG1_GL40	GL40@/KALG1@/KAL90_G0_90+@
KAL90+_GL40	GL40@/KAL90_H0_90+@/KAL90_90+@/KAL90_G0_90+@
KAL90+_GM45	GM45@/KAL90_H0_90+@/KAL90_90+@/KAL90_G0_90+@
KALH0+_GL40	GL40@/KAL90_H0_90+@/KALH0@
KALH0+_GM45	GM45@/KAL90_H0_90+@/KALH0@

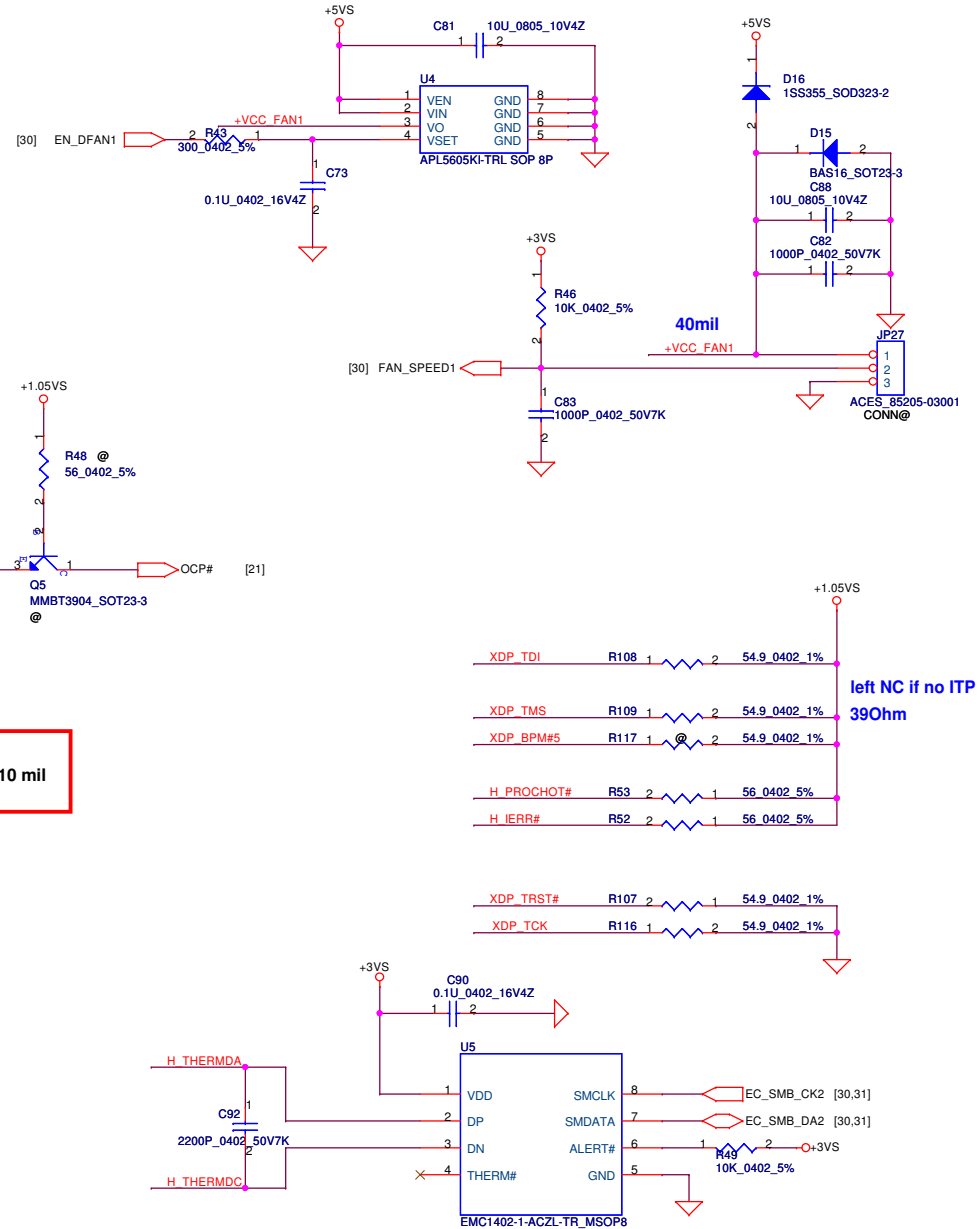
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[7] H_A# [3..35]  H_A# [3..35]
 [7] H_REQ# [0..4]  H_REQ# [0..4]
 [7] H_RS# [0..2]  H_RS# [0..2]

FAN1 Conn

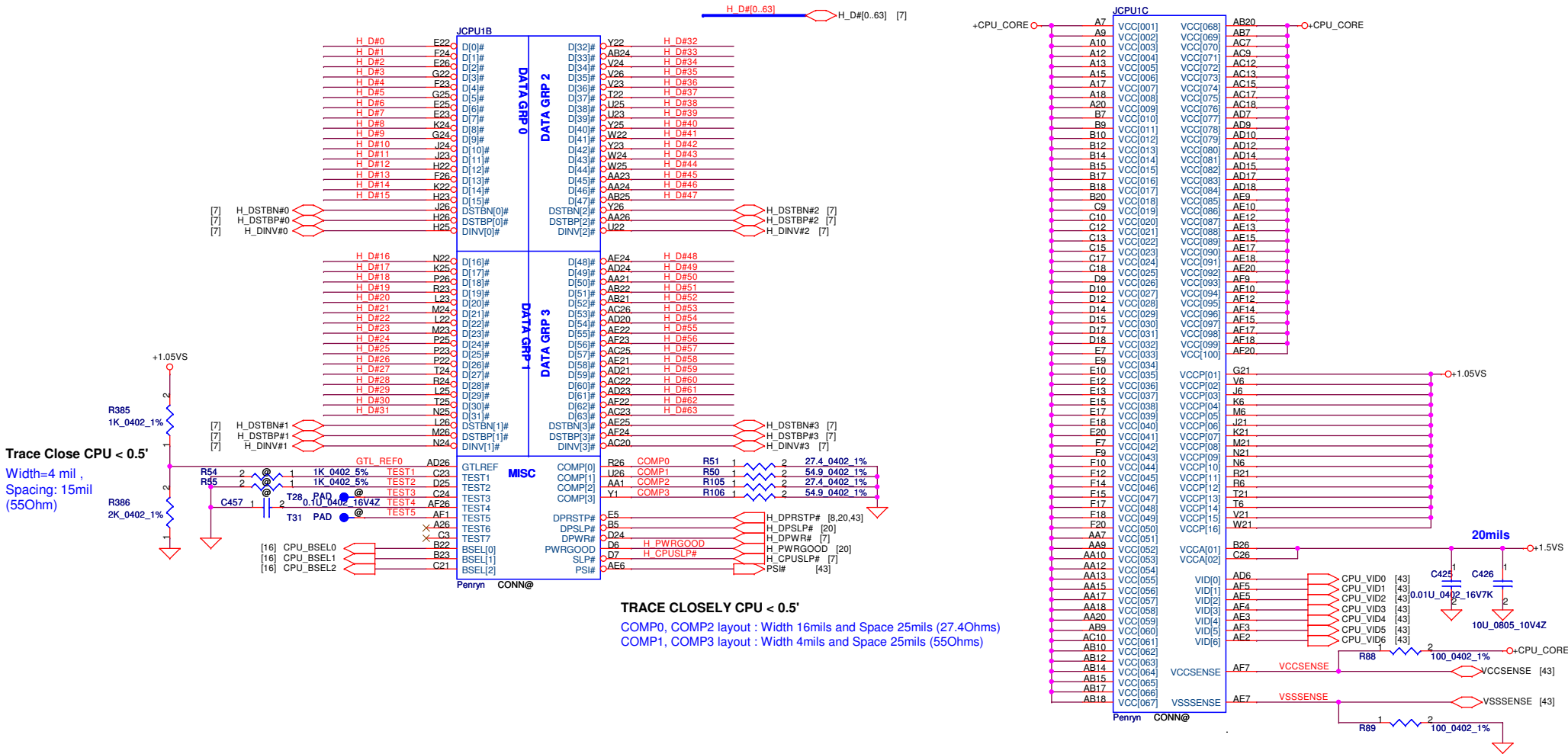


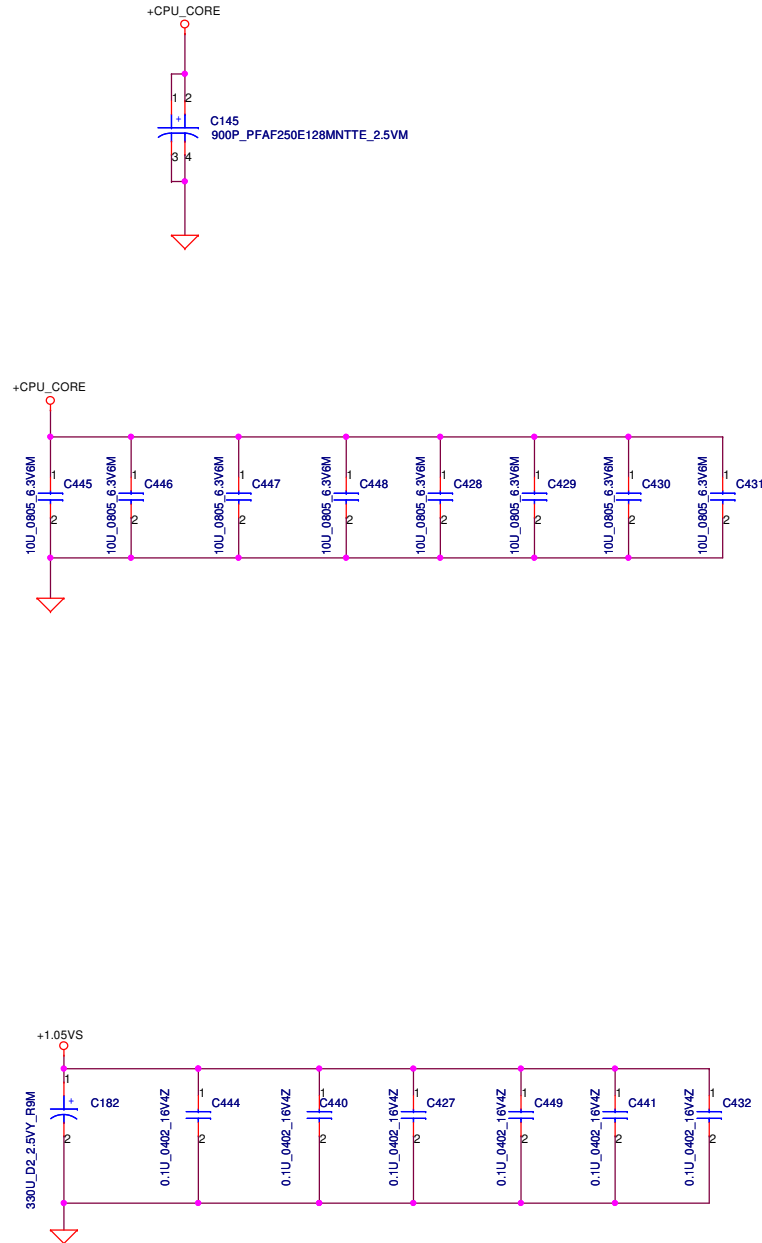
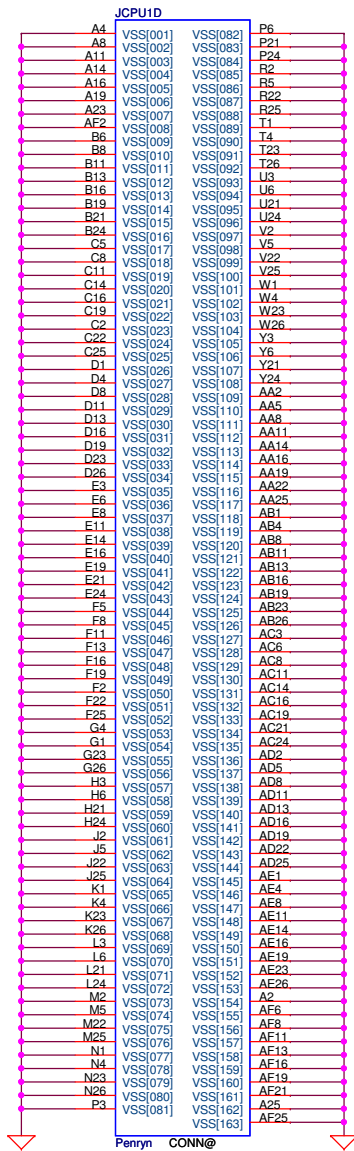
Layout Note:
H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil



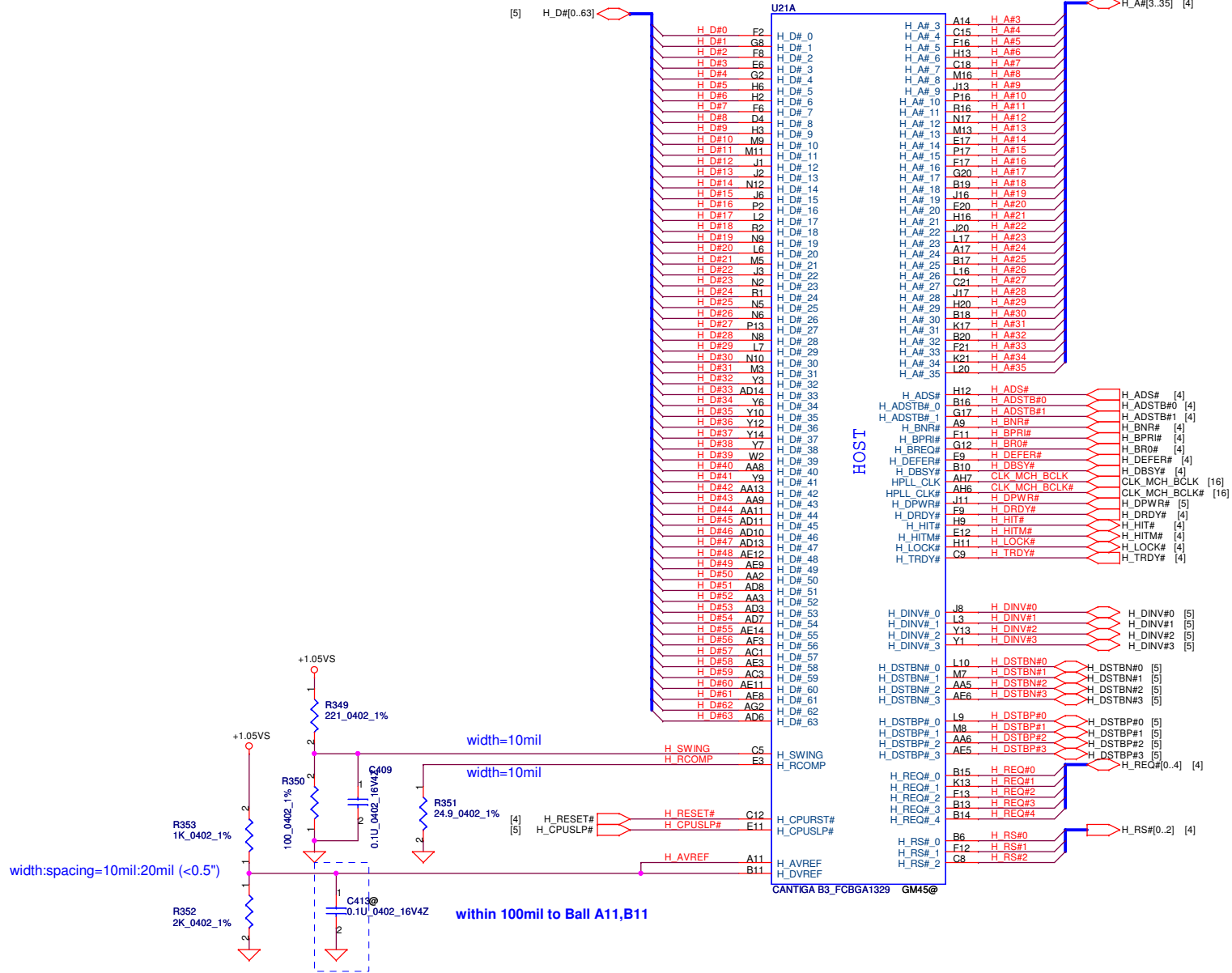
BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

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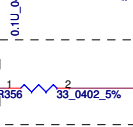
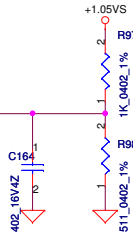
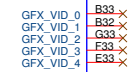
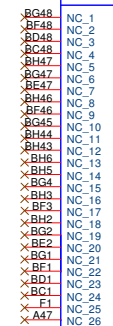
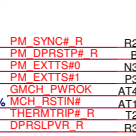
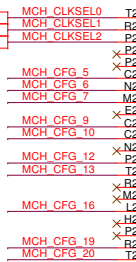
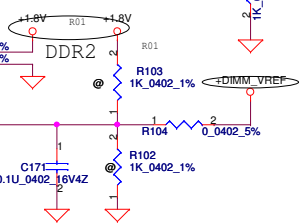
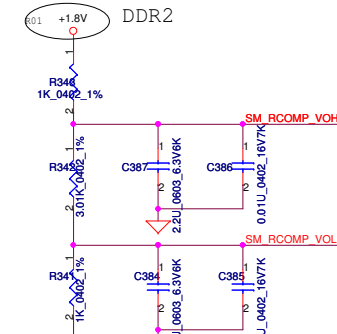




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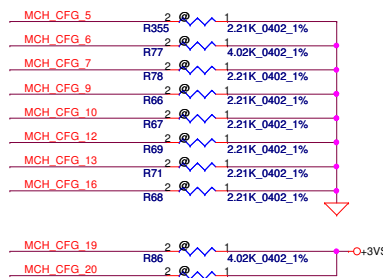


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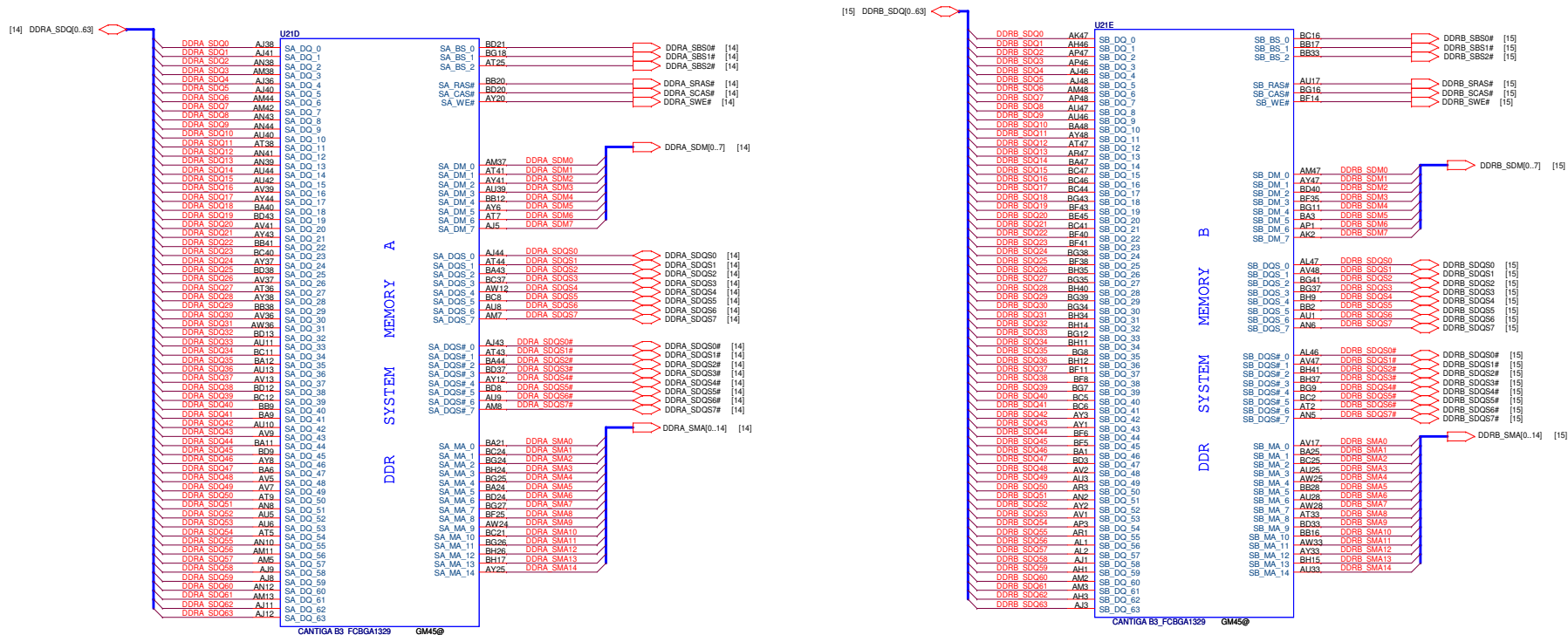
Strap Pin Table

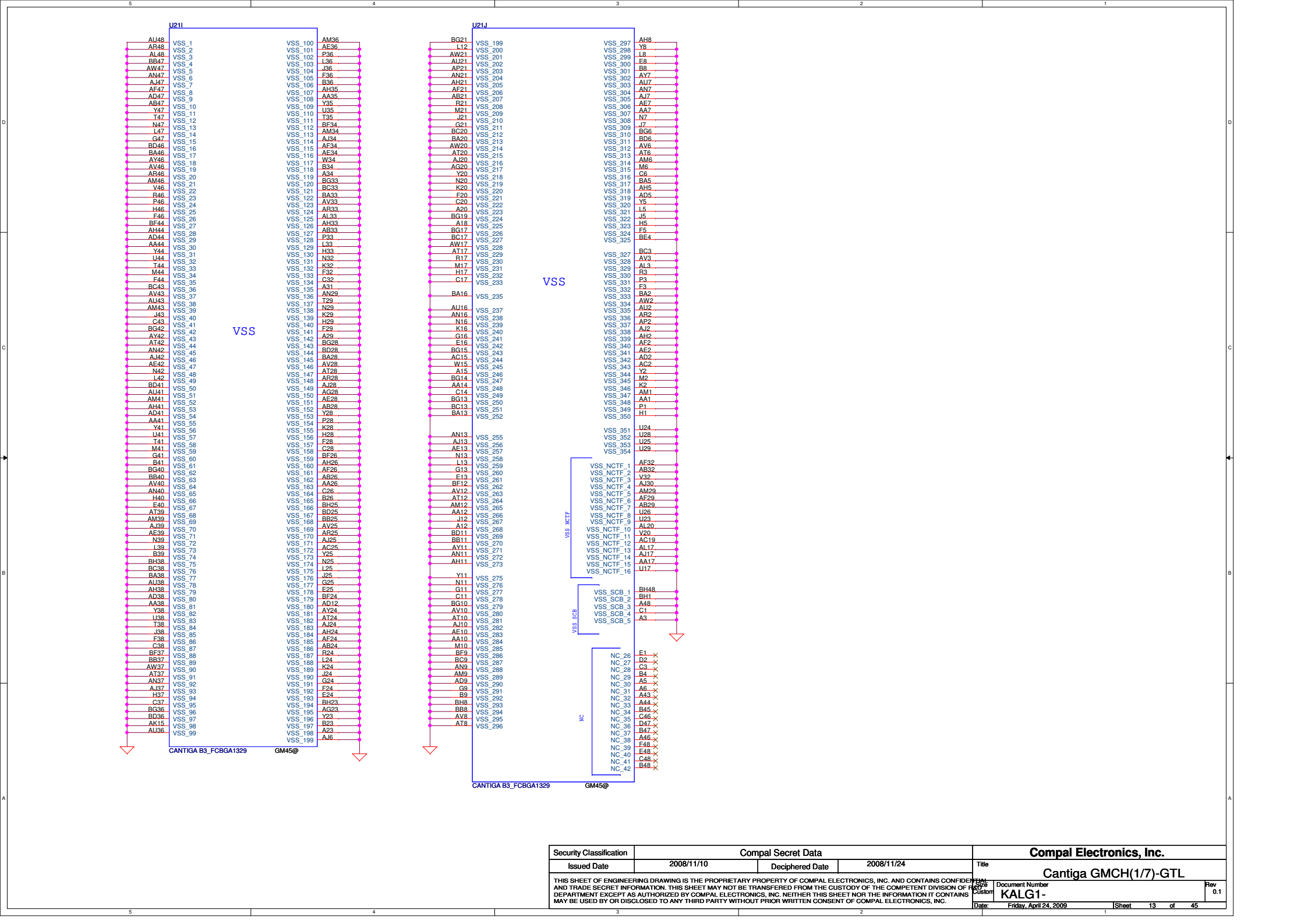
CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XDP Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. * (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable 1 = LFP Card Present; PCIe disable * (Default)
DDPC_CTRLDATA	0 = Digital DisplayPort Disable 1 = Digital DisplayPort Device Present * (Default)



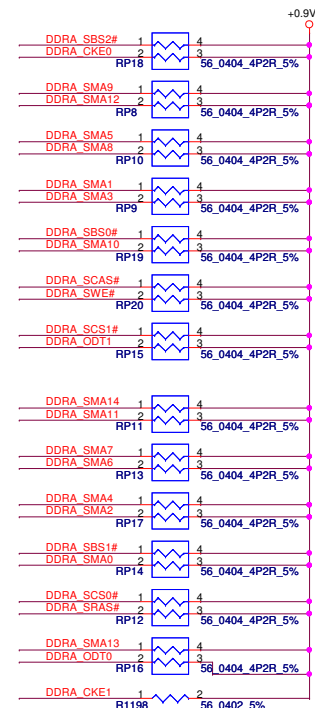
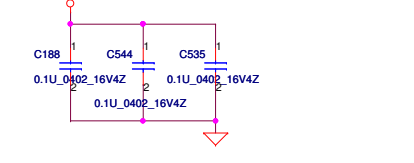
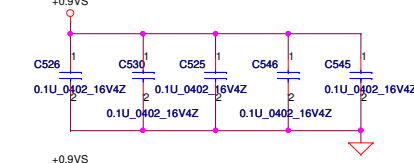
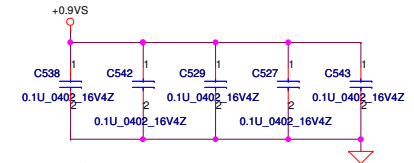
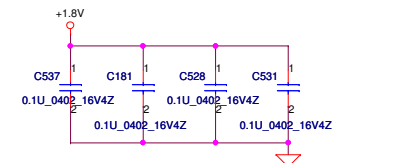
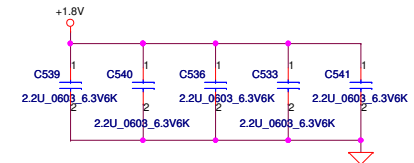
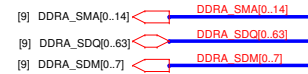
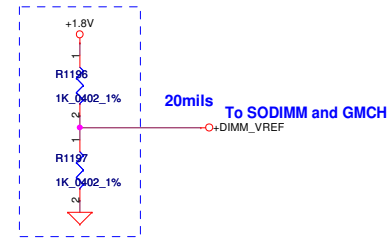
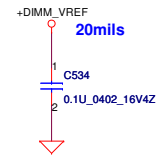
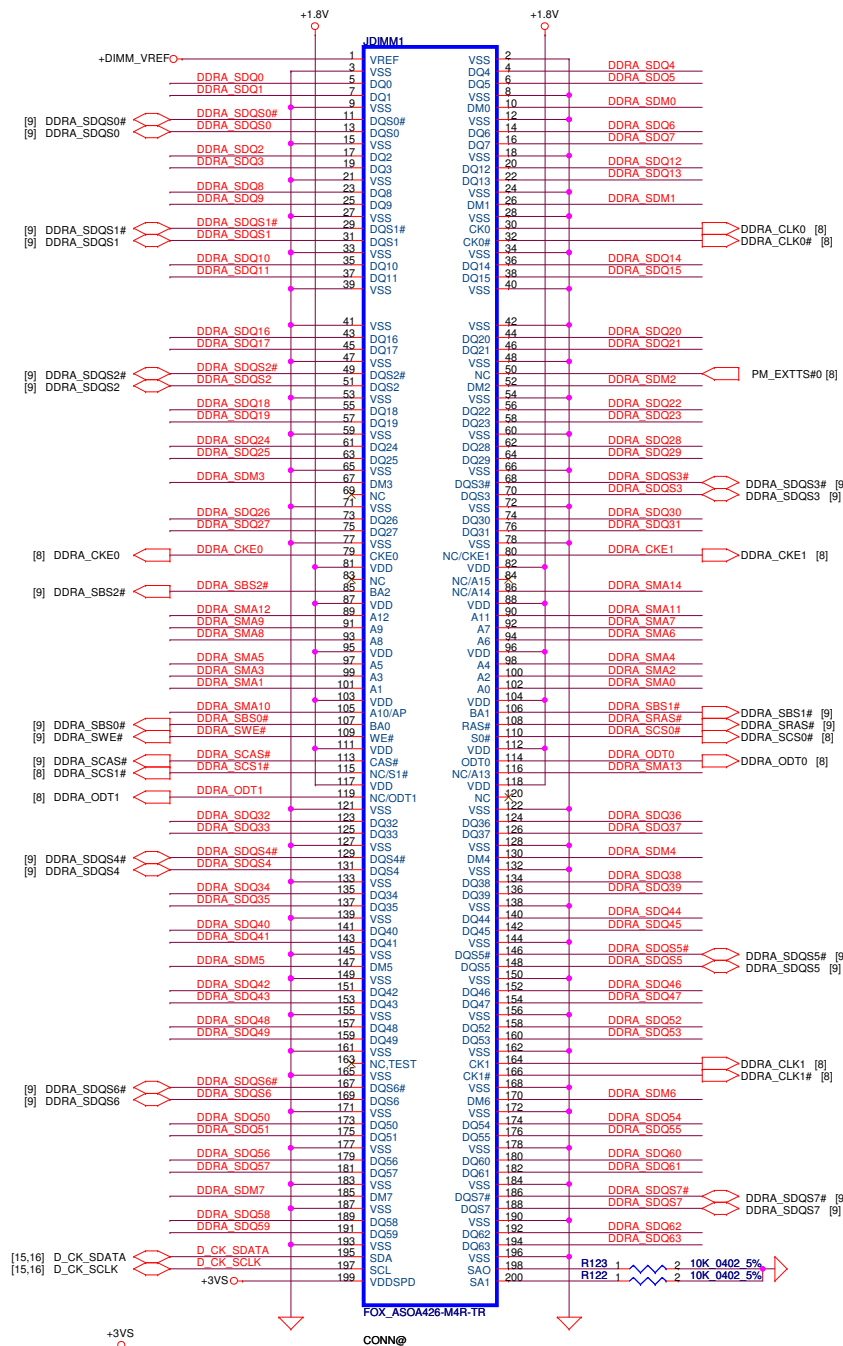
Notice: Please check HDA power rail to select HDA controller

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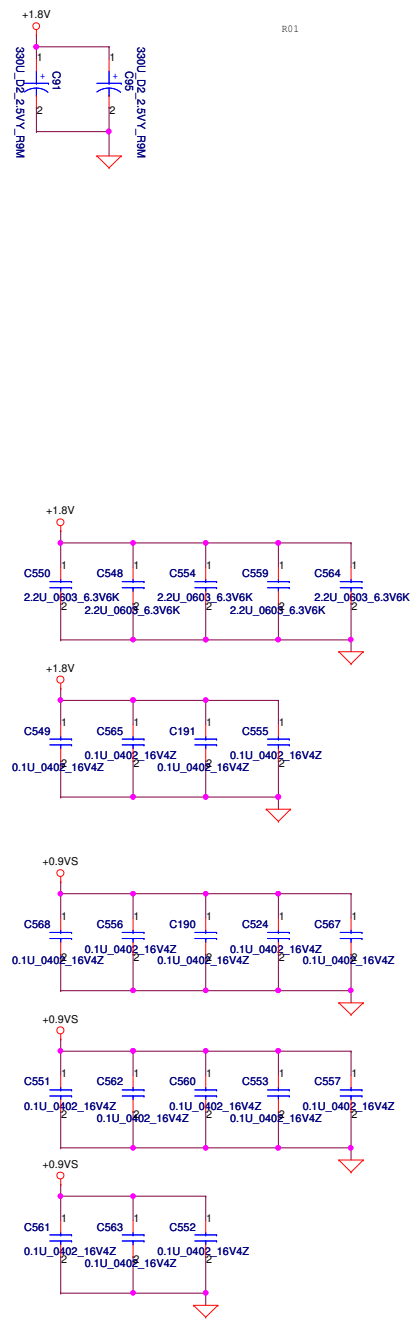
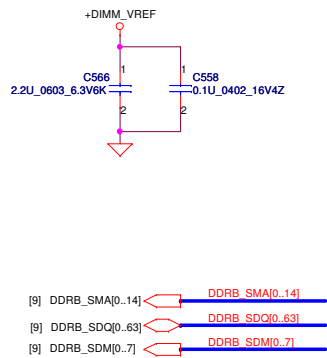
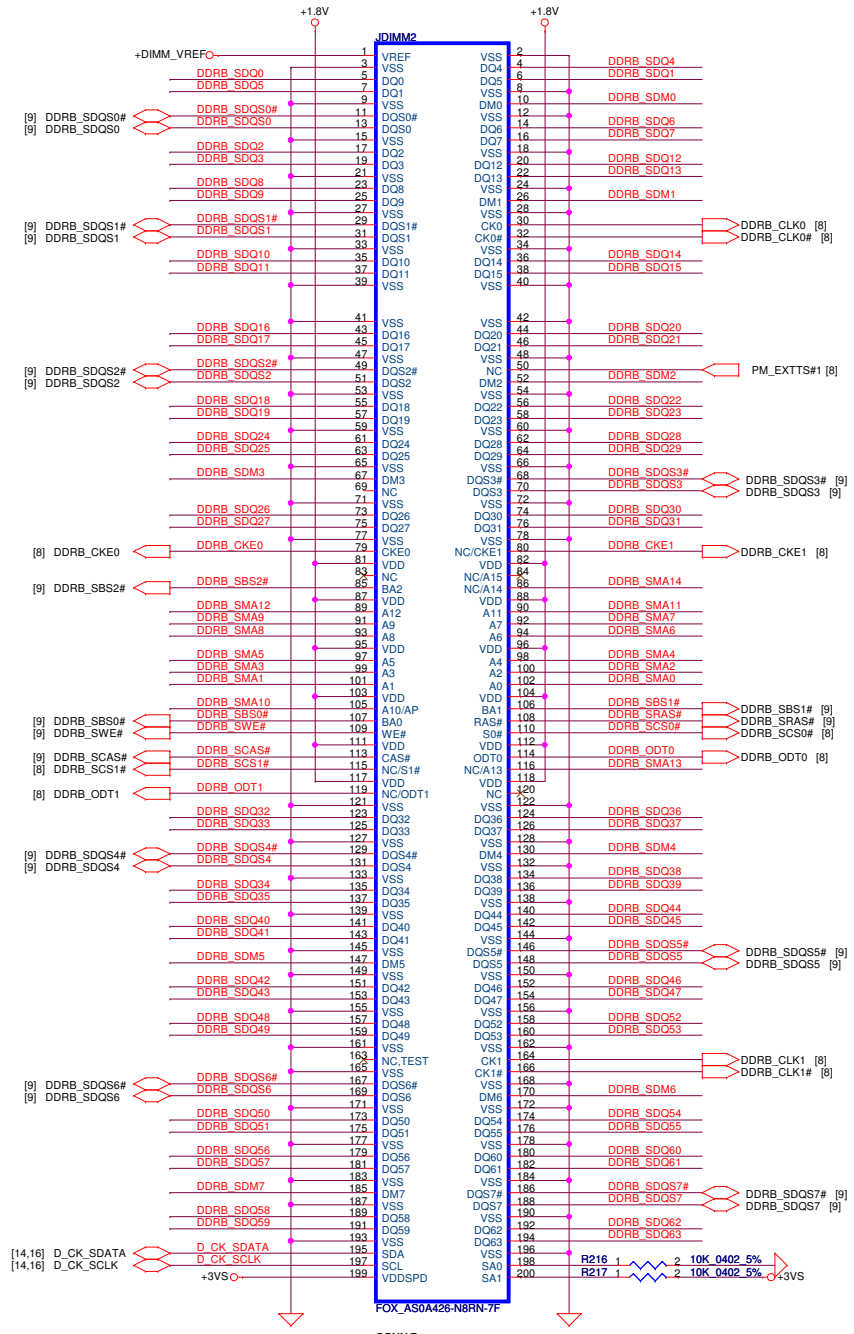
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DIMM1 REV H:5.6mm (BOT)

JDIMM1 --- Change to low size

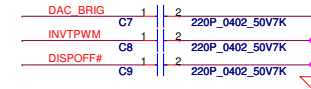
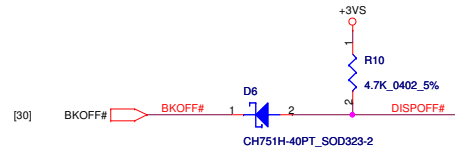
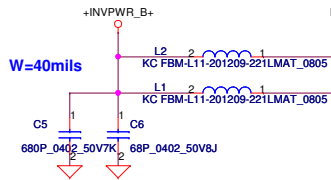
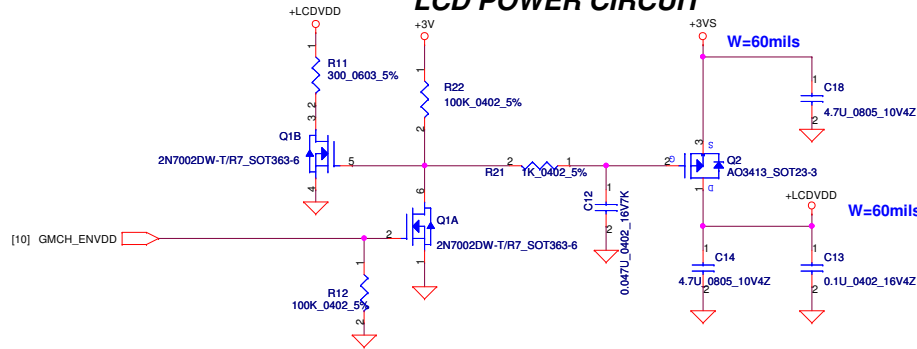
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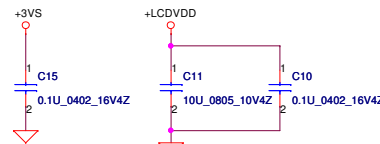
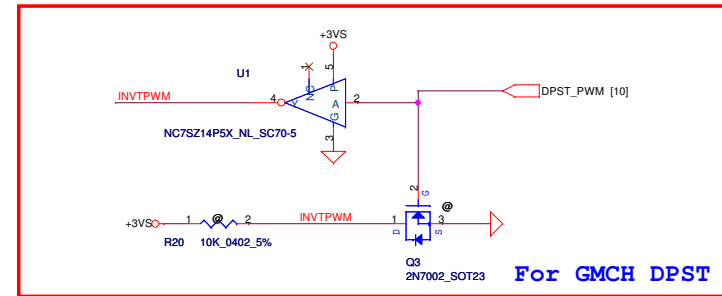
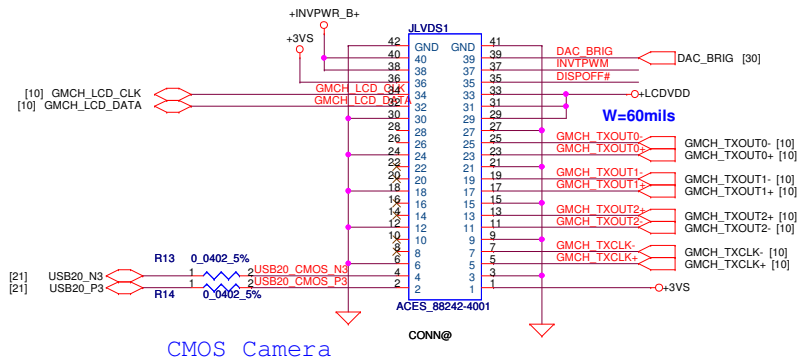
DIMM2 REV H:9.2mm (BOT)
JDIMM2 --- Change to high size

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LCD POWER CIRCUIT

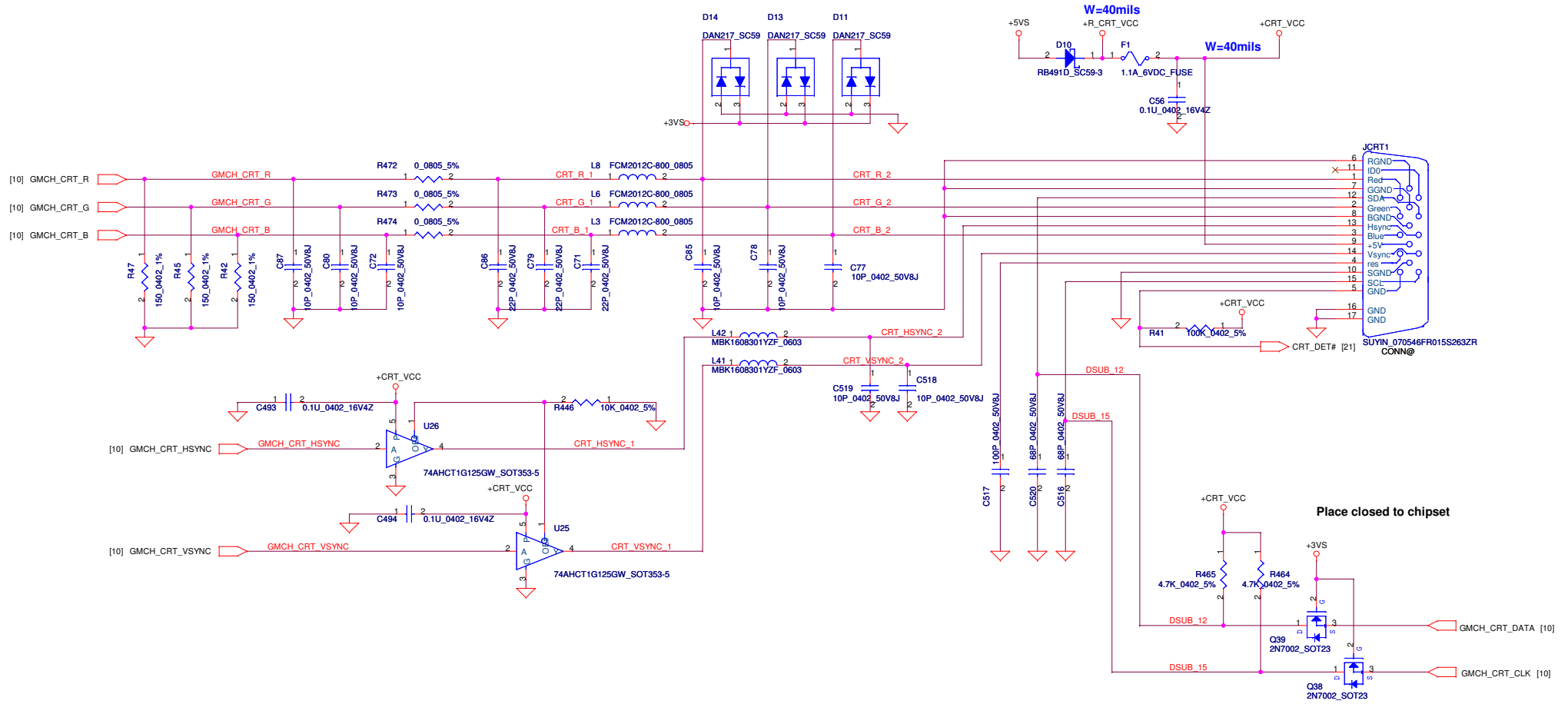


LCD/PANEL BD. Conn.

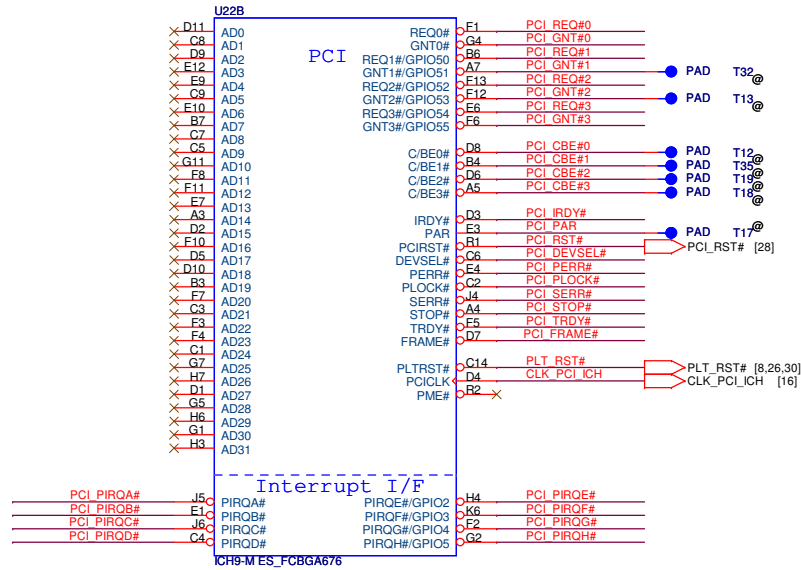
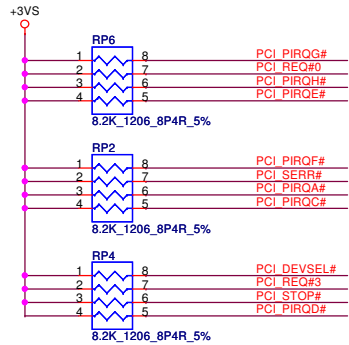
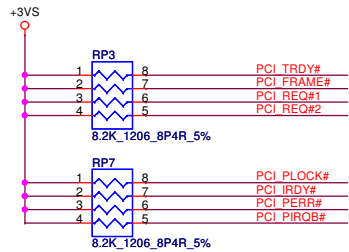


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				KALG1-	0.1
				Date: Friday, April 24, 2009	Sheet 17 of 45

CRT Connector

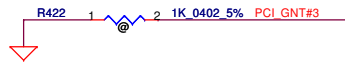


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Issued Date		2008/11/10		Deciphered Date		2008/11/24		Title			
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								Document Number		Rev	
								KALG1-		0.1	
								Date		Friday, April 24, 2009	
				Sheet		18		of 45			

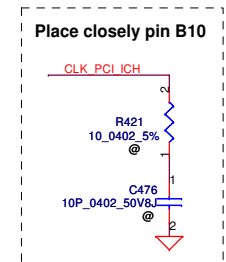
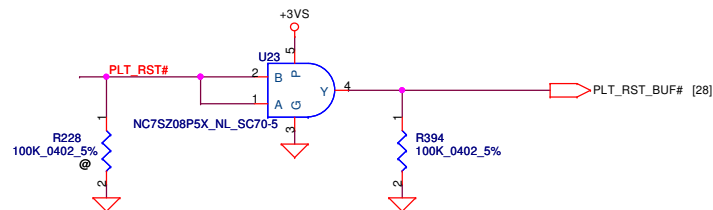
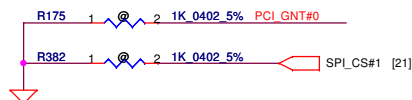


DMI for ESI-compatible operation
PCI_GNT#1 Low= DMI for ESI-compatible operation
 High= Default* (Internal pull-up)

A16 Swap Override Strap
PCI_GNT#3 Low= A16 swap override Enable
 High= Default*



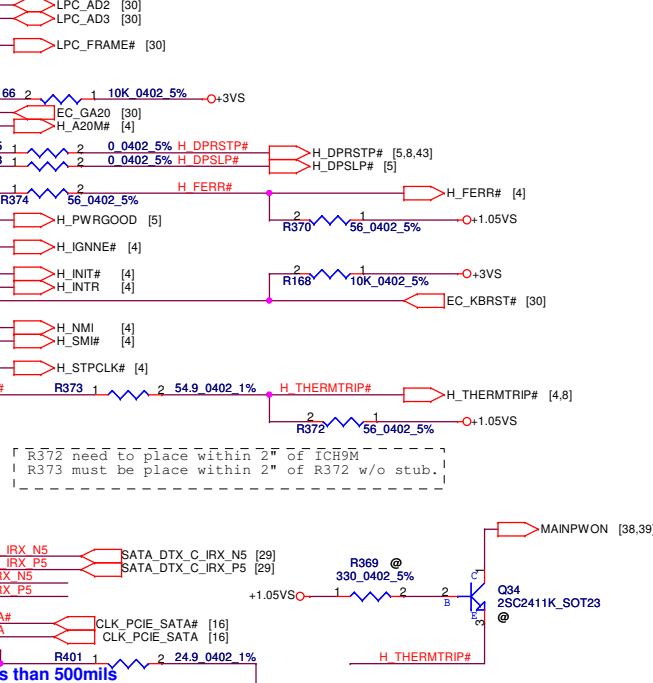
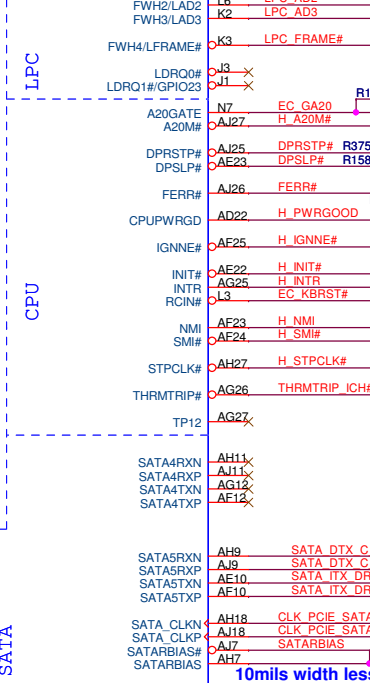
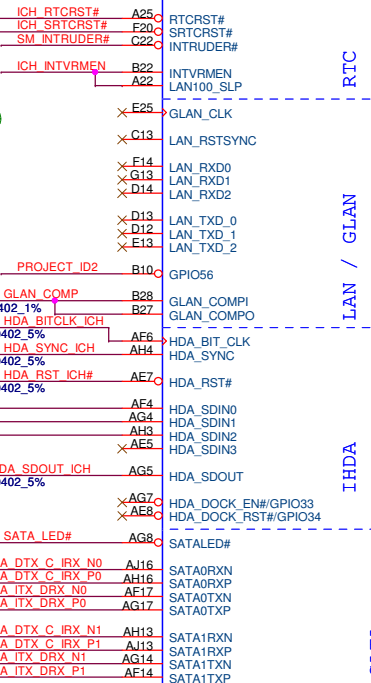
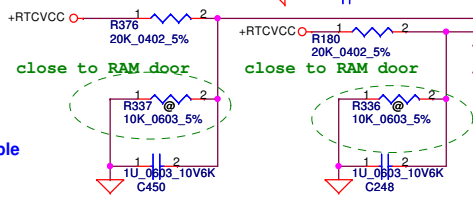
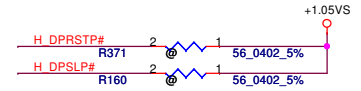
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



CMOS Settings	R337
Clear CMOS	SHORT
Keep CMOS	OPEN

TPM Settings	R336
Clear ME RTC Registers	SHORT
Keep ME RTC Registers	OPEN

Reset r1290 for power on then shut down issue



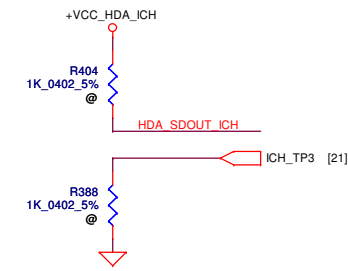
SATA for HDD

SATA for ODD

HDA for AUDIO

HDA for GMCH

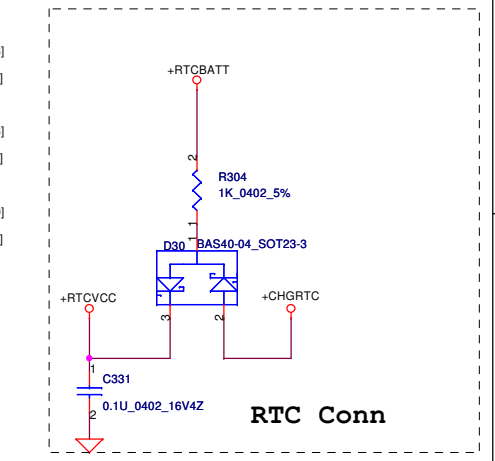
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KAL90+	1	0	0
KALG1	0	1	0
KALG0	1	1	0
KALG1_H0+	0	0	1
KALG1_90+	1	0	1



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIe port config bit 1

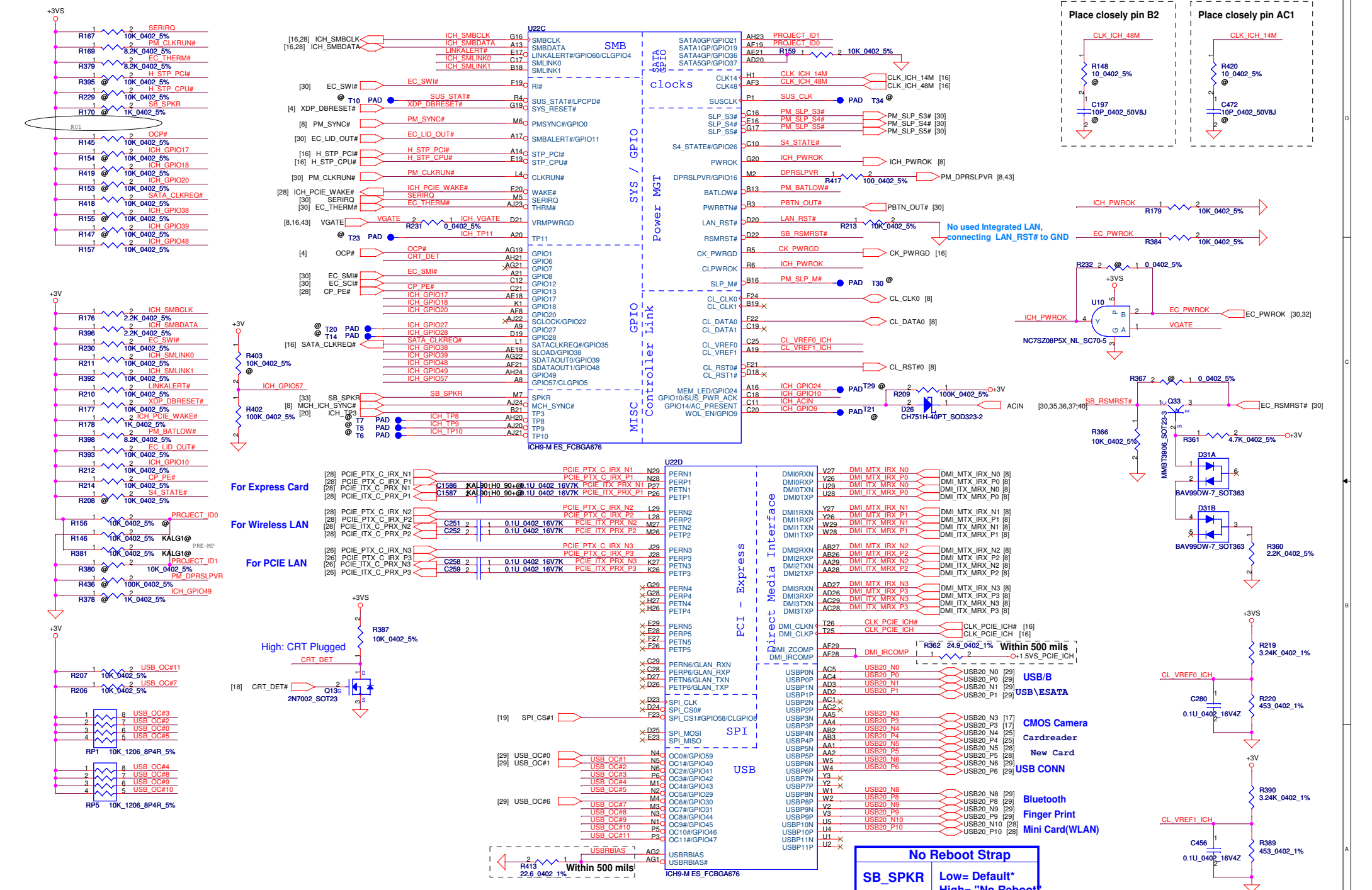
Flash Descriptor Security Override Strap
GPIO33 Low= Descriptor Security override
High= Default* (Internal pull-up)

Security Classification	Compal Secret Data
Issued Date	2008/11/10
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Compal Electronics, Inc.	
Title ICH9M(2/4)-LAN, IDELPC, RTC	
Size Custom	Document Number KALG1-
Date: Friday, April 24, 2009	Sheet 20 of 45

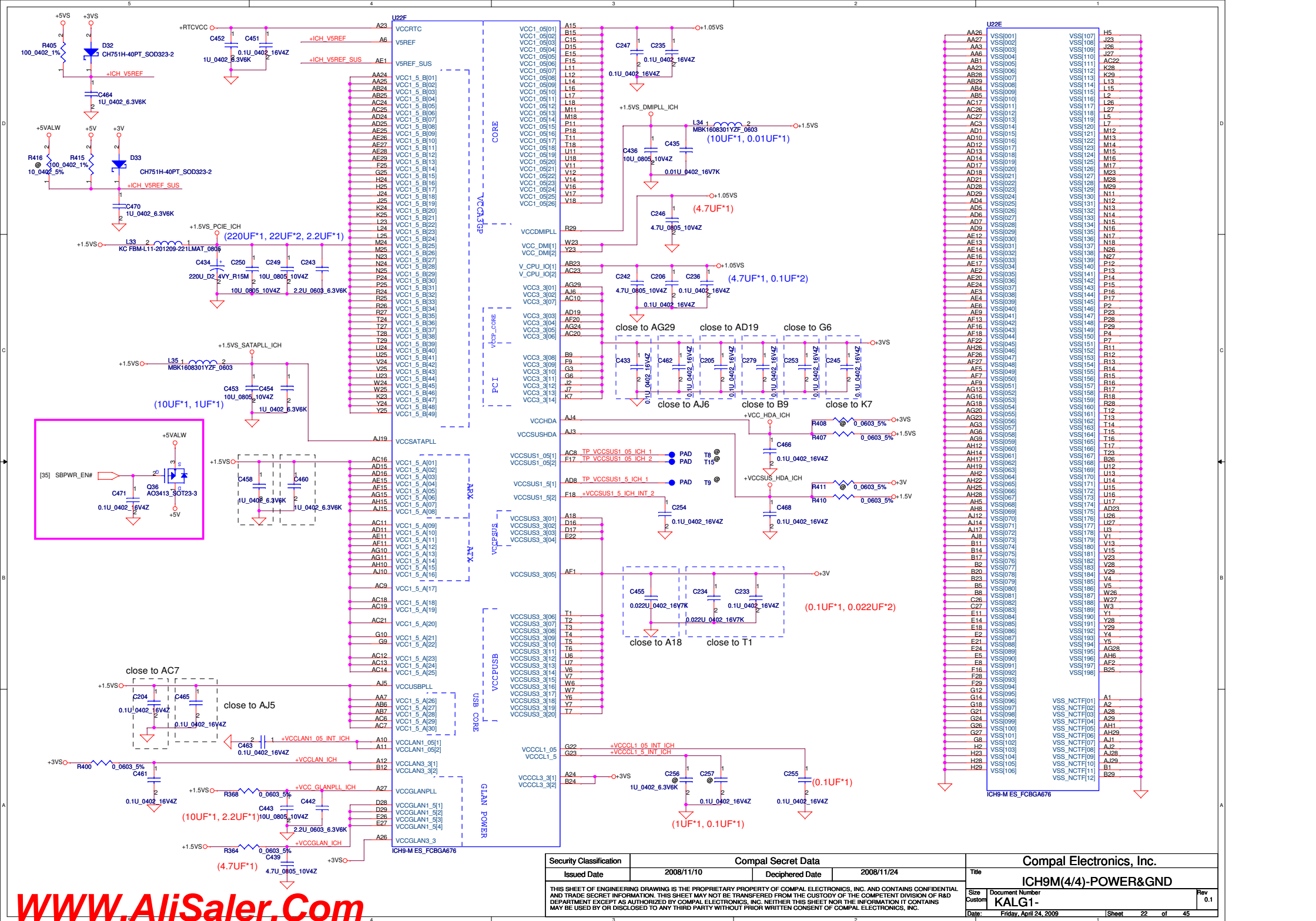
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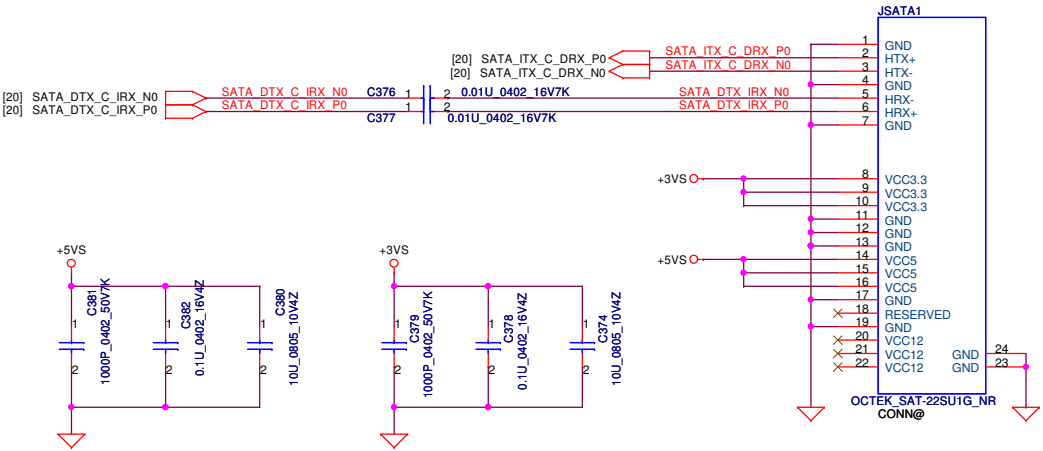
Internal TPM Strap		DMI Termination Voltage	
SPI_MOSI	Low= Disable* High= ITPM enable by MCH strap	GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

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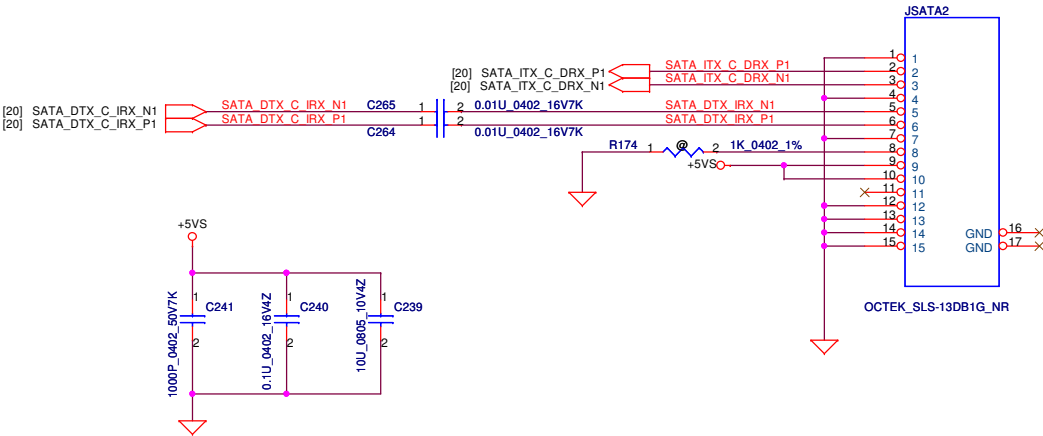
Compal Electronics, Inc.		ICH9M(3/4)-USB,GPIO,PCIE	
Customer	Document Number	Rev	0.1
KALG1-			
Date	Friday, April 24, 2009	Sheet	21 of 45



SATA HDD Conn.

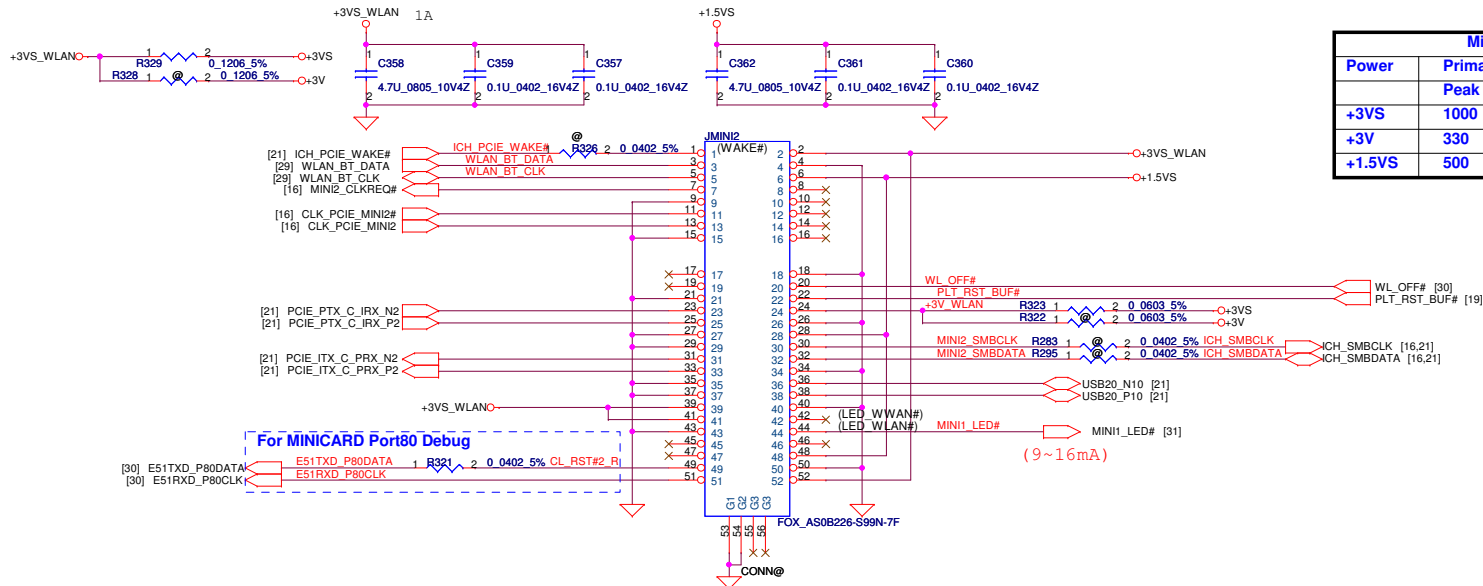


SATA ODD Conn.



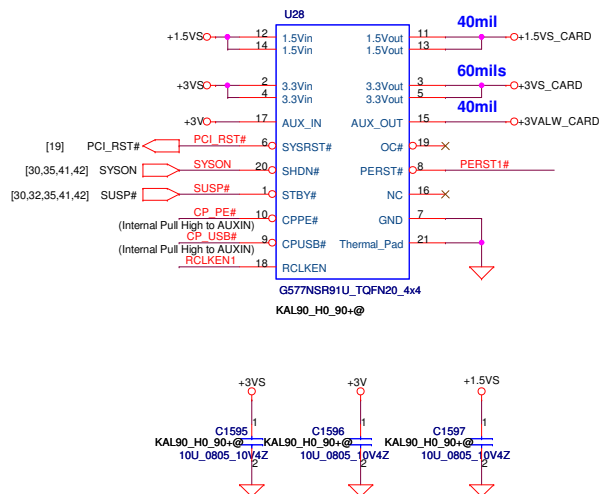
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Issued Date		2008/11/10		Deciphered Date		2008/11/24		Title			
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						Size	Document Number			Rev	
						Custom	KALG1-			0.1	
						Date:	Friday, April 24, 2009		Sheet 23 of 45		

For Wireless LAN

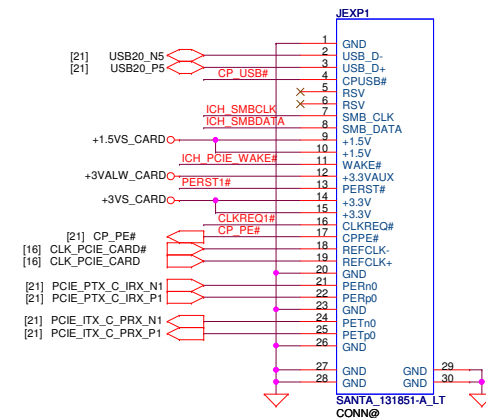


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

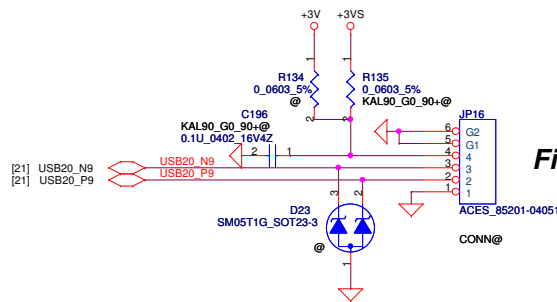
New Card Power Switch



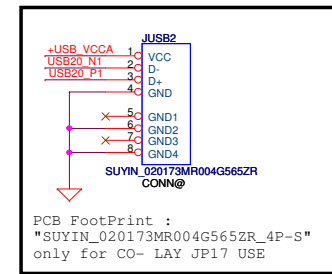
New Card Socket (Left/TOP)



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				Document Number				KALG1-			
				Rev				0.1			
				Sheet				28 of 45			

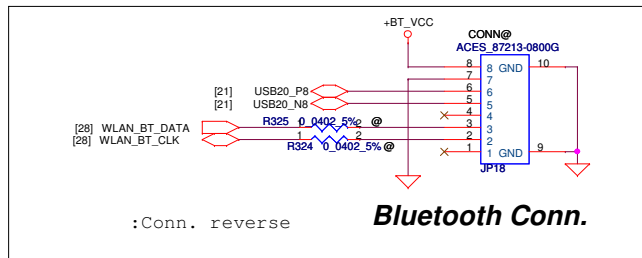
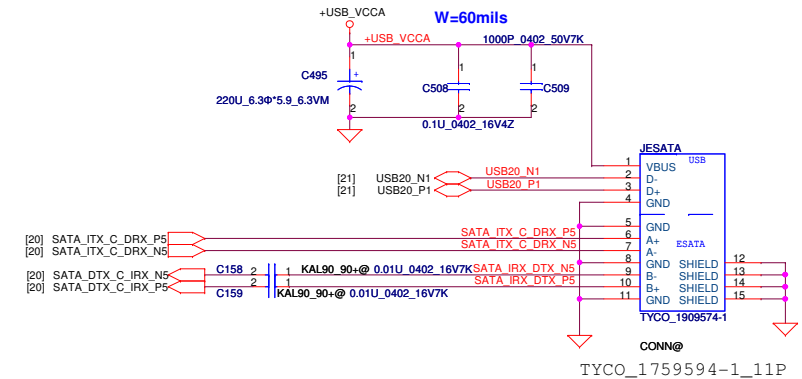
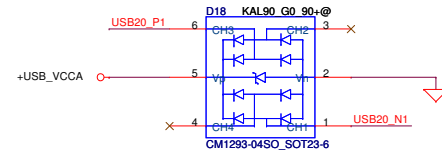
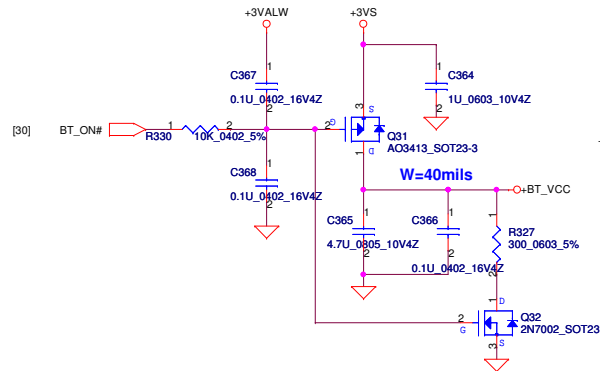


Finger Print Conn.



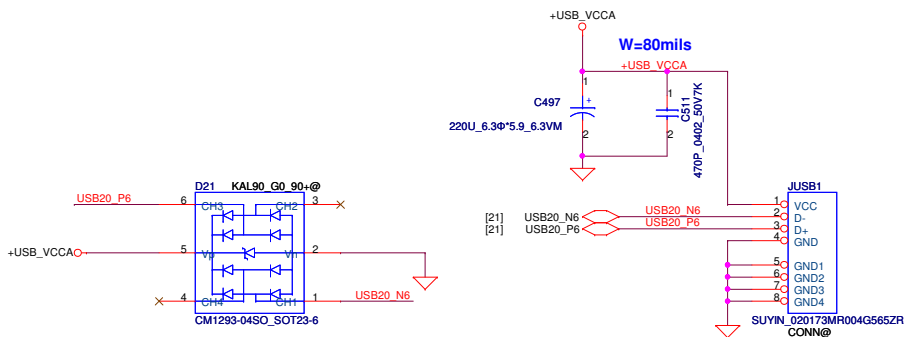
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only for CO- LAY JP17 USE

ESATA CONN

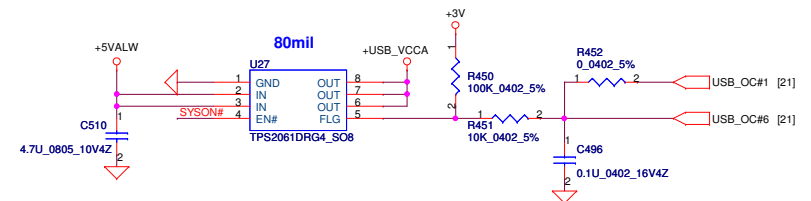


Bluetooth Conn.

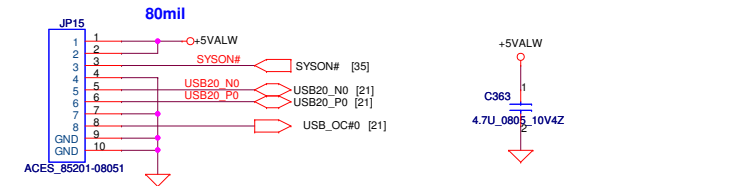
:Conn. reverse



USB CONN.

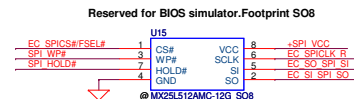


To USB/B Connector

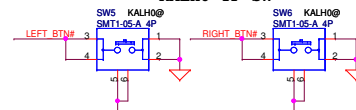
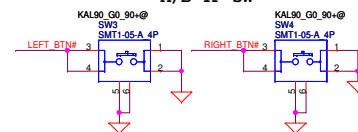
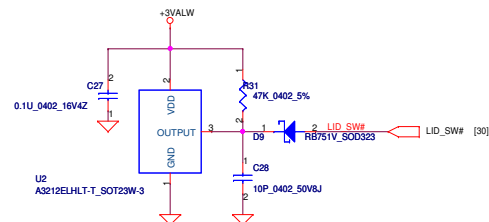
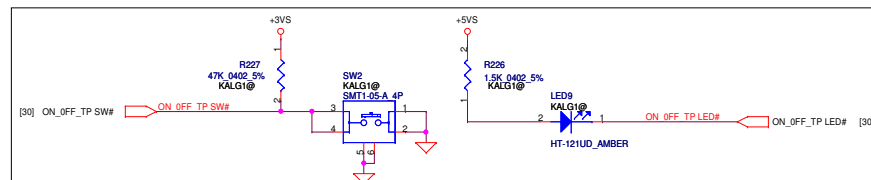
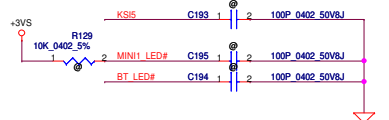
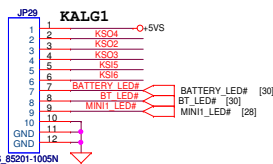
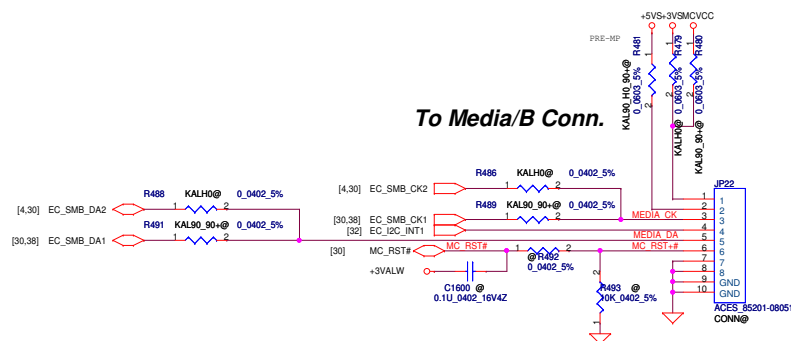
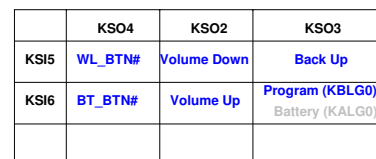
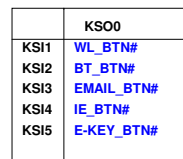
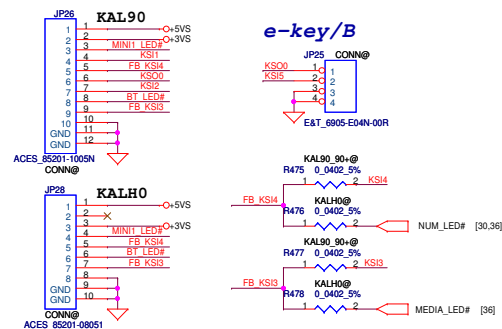


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								Document Number		KALG1-		Rev		0.1	
								Date		Friday, April 24, 2009		Sheet		29 of 45	



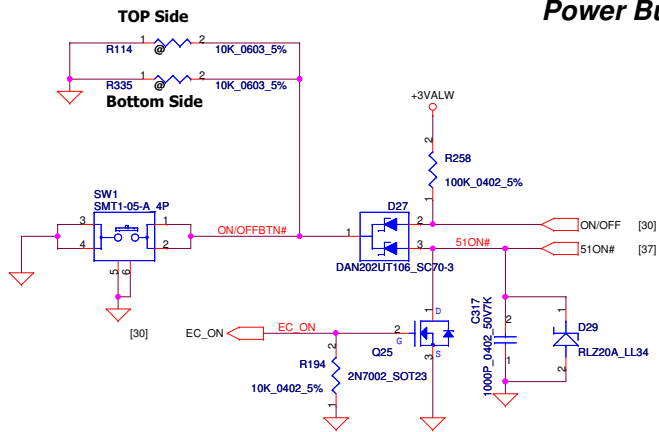


To TP/B Conn.

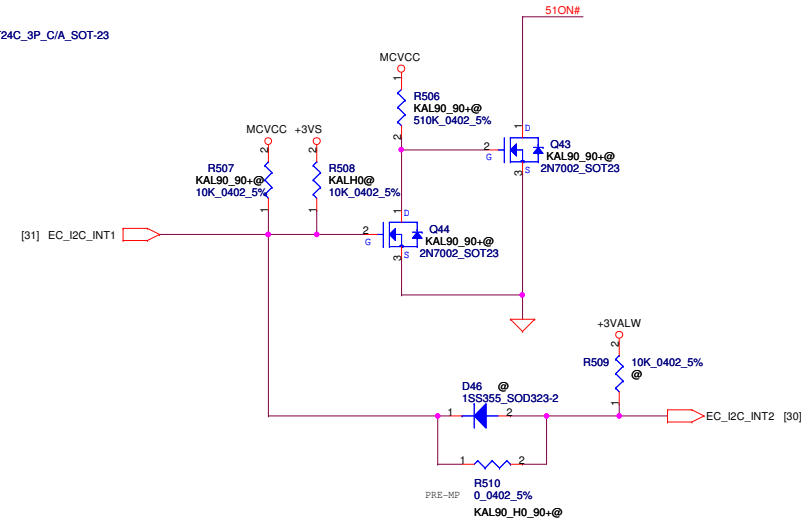
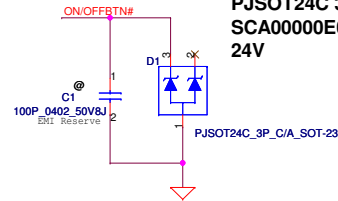

$$e\text{-key}/B$$


	Compar Electronics, Inc.
Title	BIOS, I/O Port & K/B Connector

Power Button

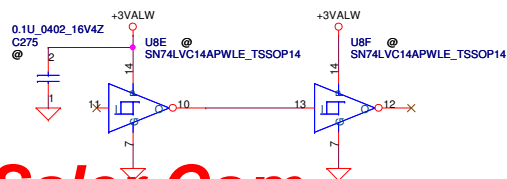
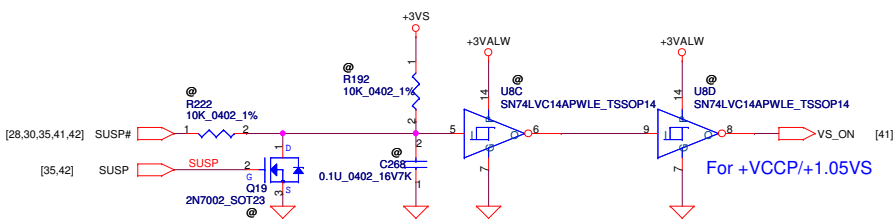
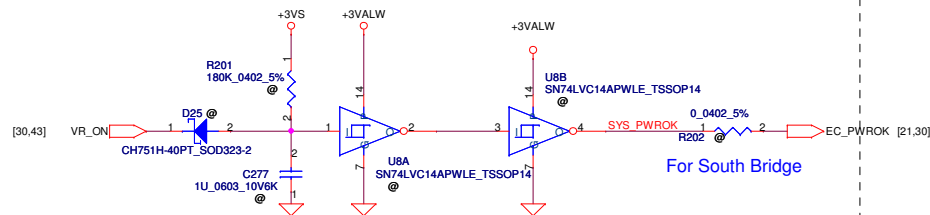
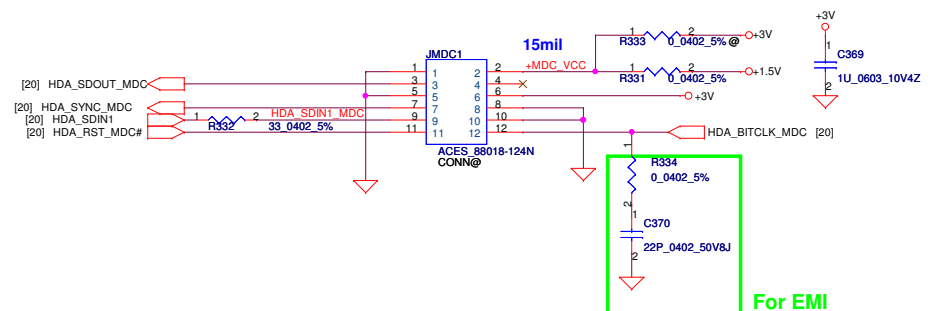


D58 USE
PJSOT24C 3P C/A SOT-23
SCA00000E00
24V



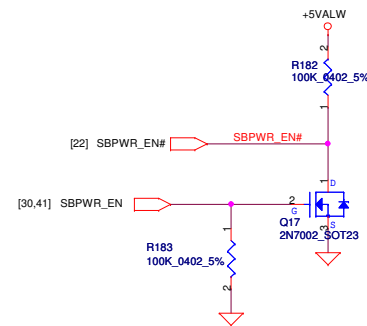
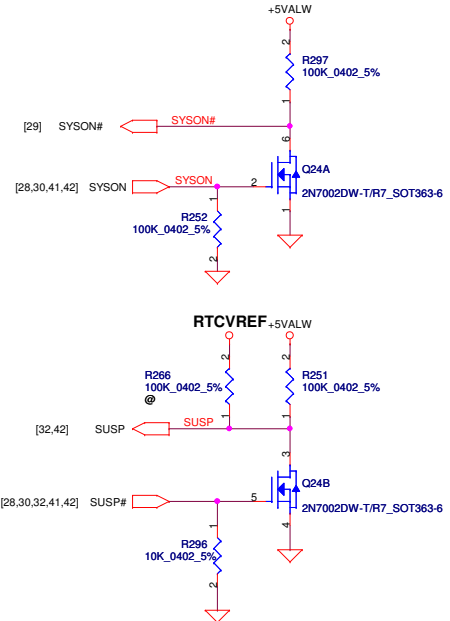
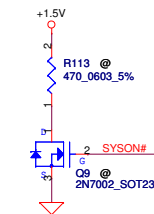
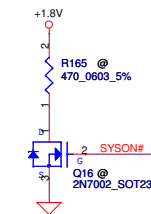
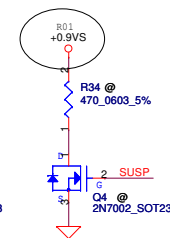
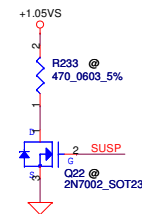
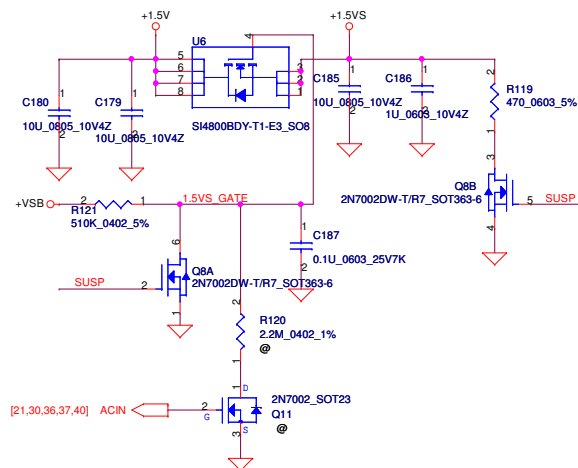
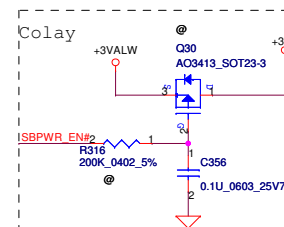
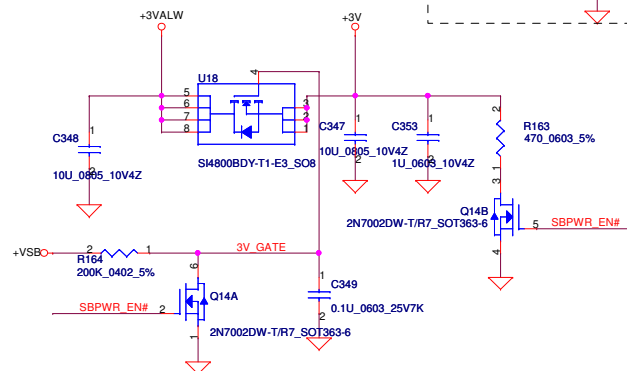
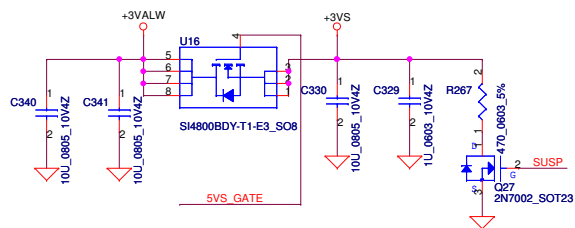
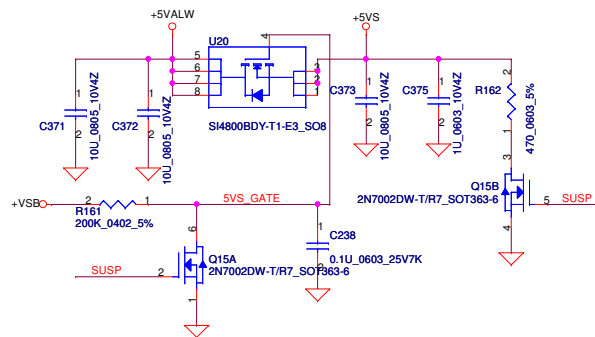
Power ON Circuit

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RESERVE R01
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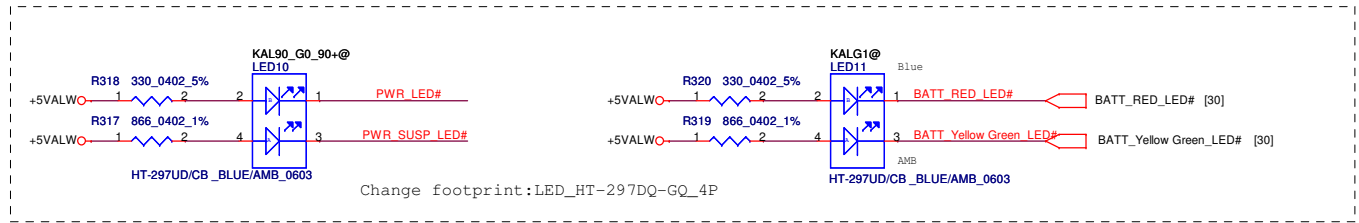
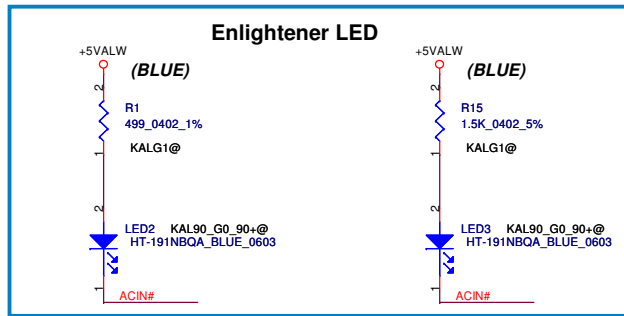
***HDA MDC Conn.***

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					KALG1-	0.1	
					Date	Friday, April 24, 2009	Sheet

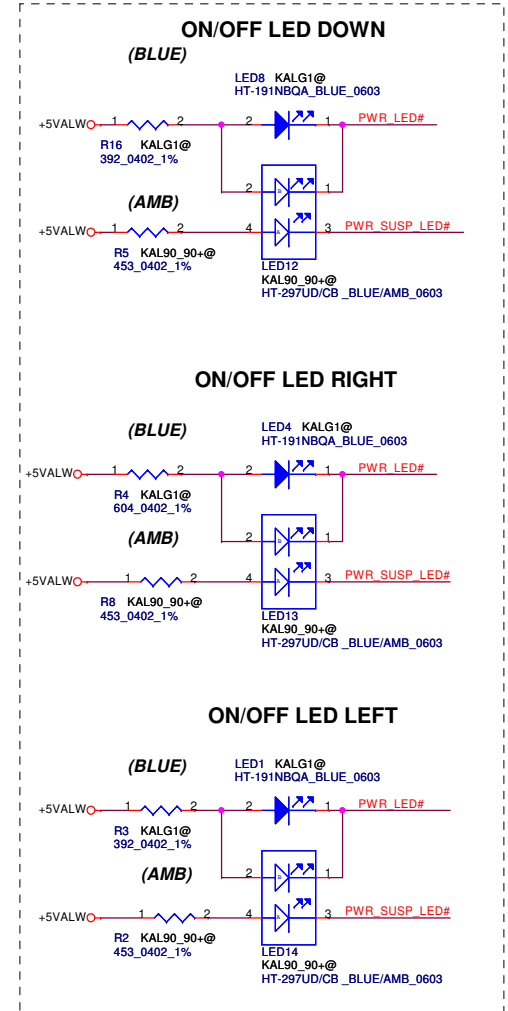
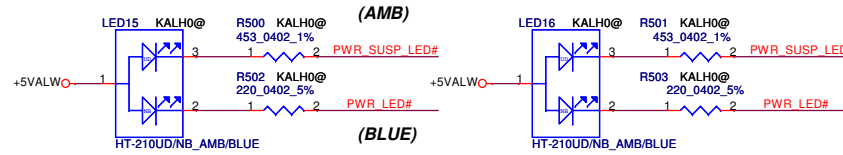
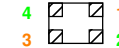
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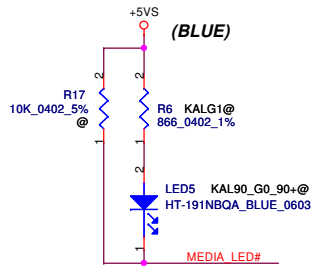
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Issued Date	2008/11/10	Deciphered Date	2008/11/24	Title	DC Interface & Screw Hole	
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				KALG1-	0.1	
				Date	Friday, April 24, 2009	Sheet 35 of 45



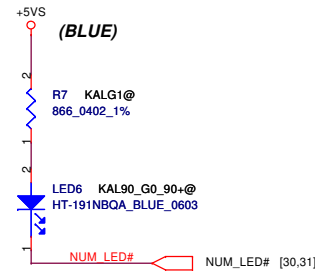
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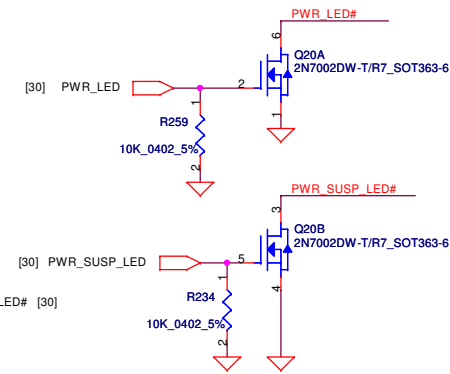
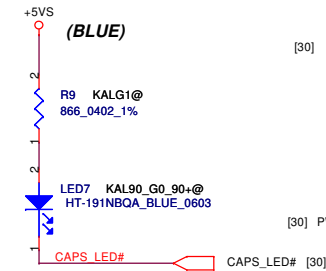
MEDIA_LED



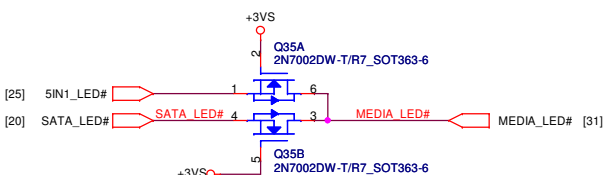
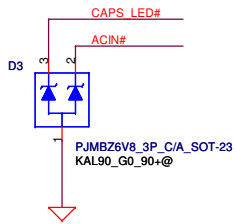
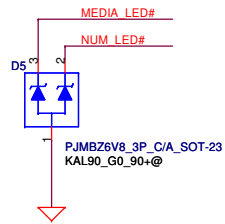
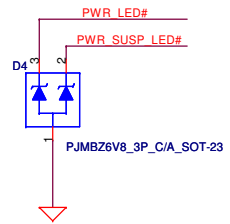
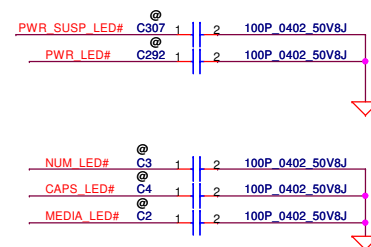
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CAPS_LED

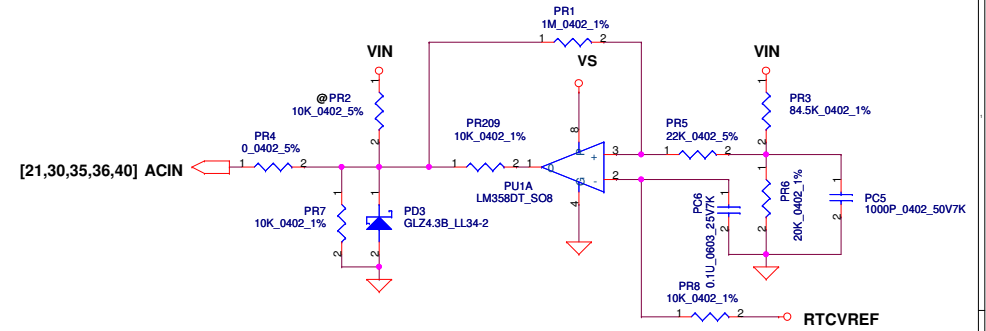
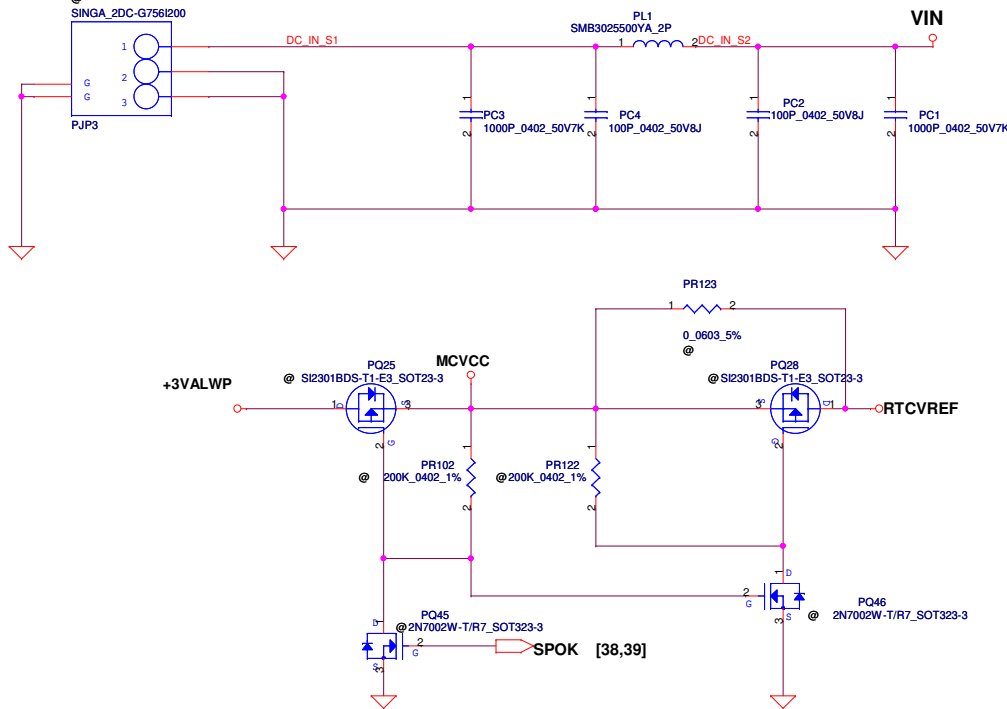


FOR EMI



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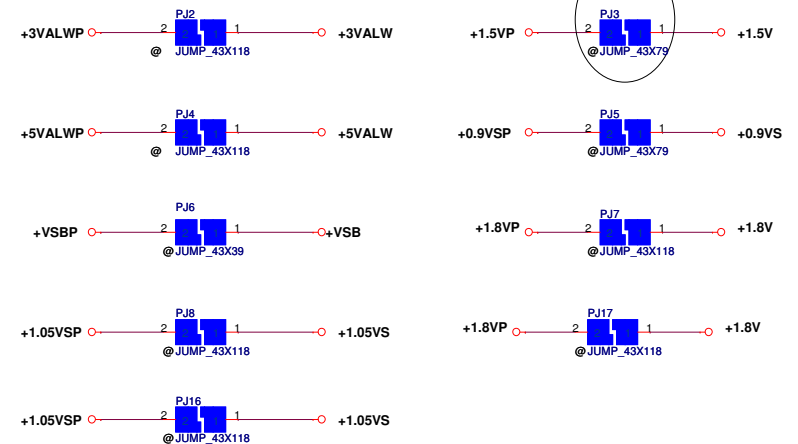
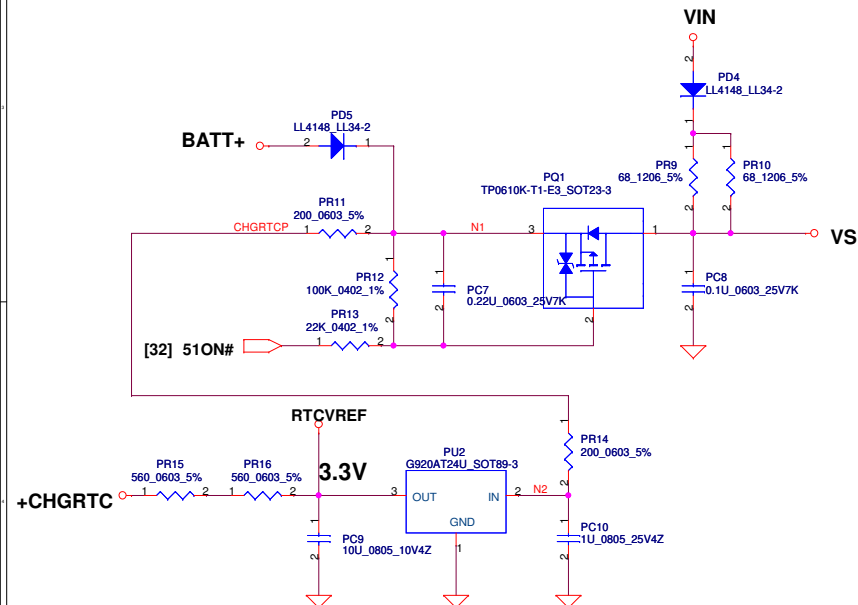
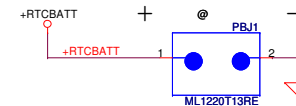
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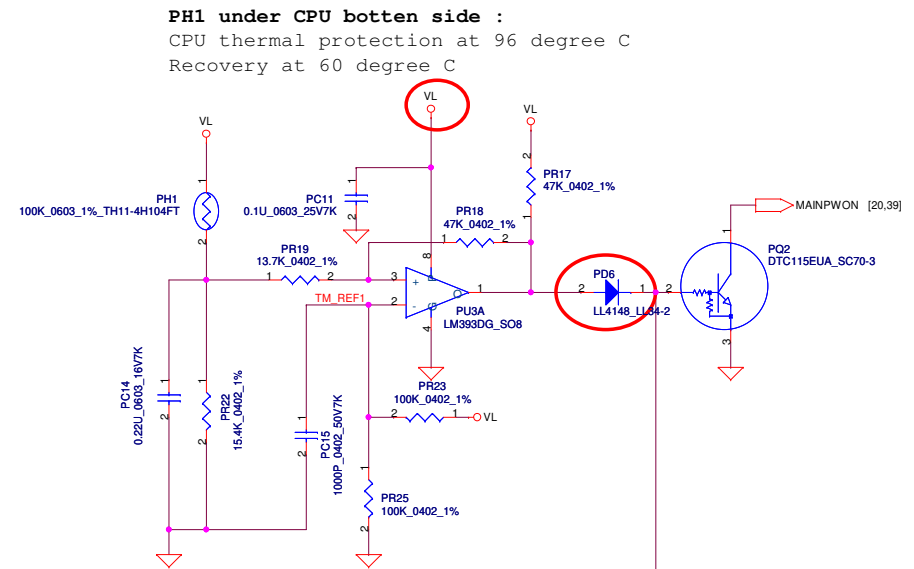
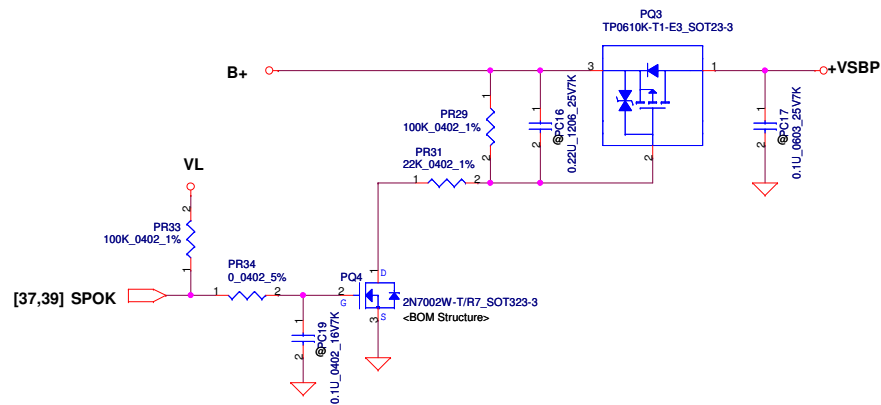
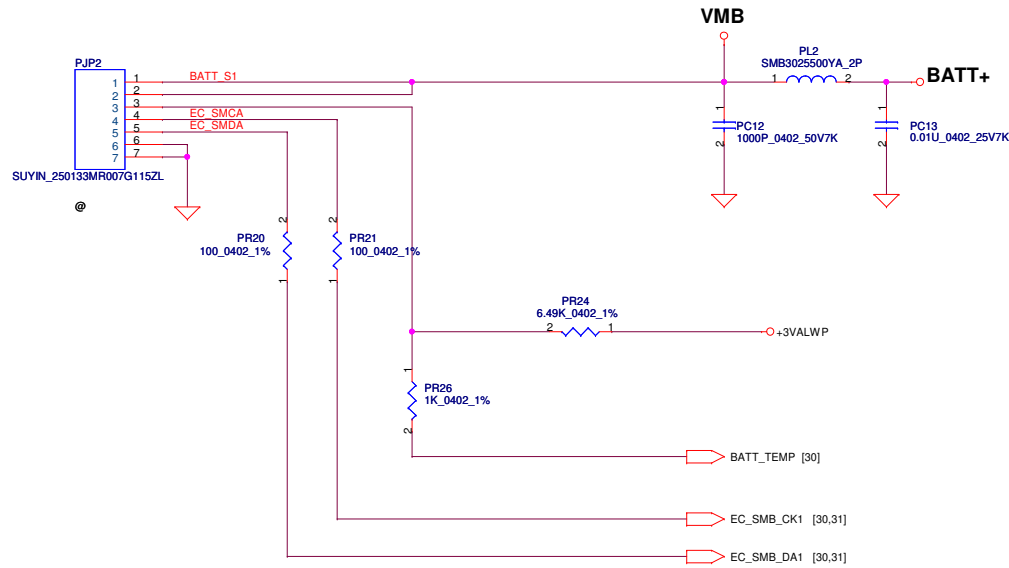
Vin Detector

	Min.	Typ	Max.
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L-->H	17.430V	17.901V	18.384V

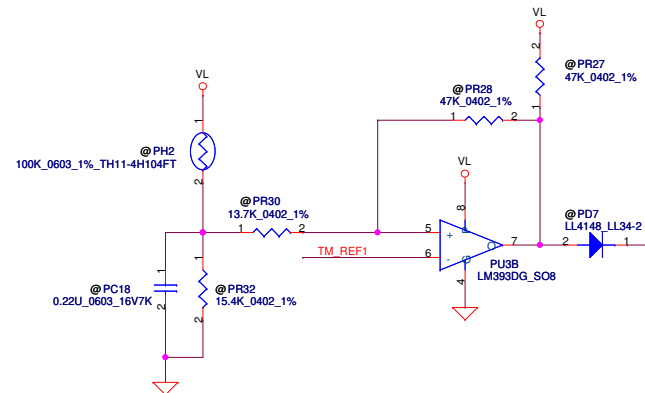
RTC Conn



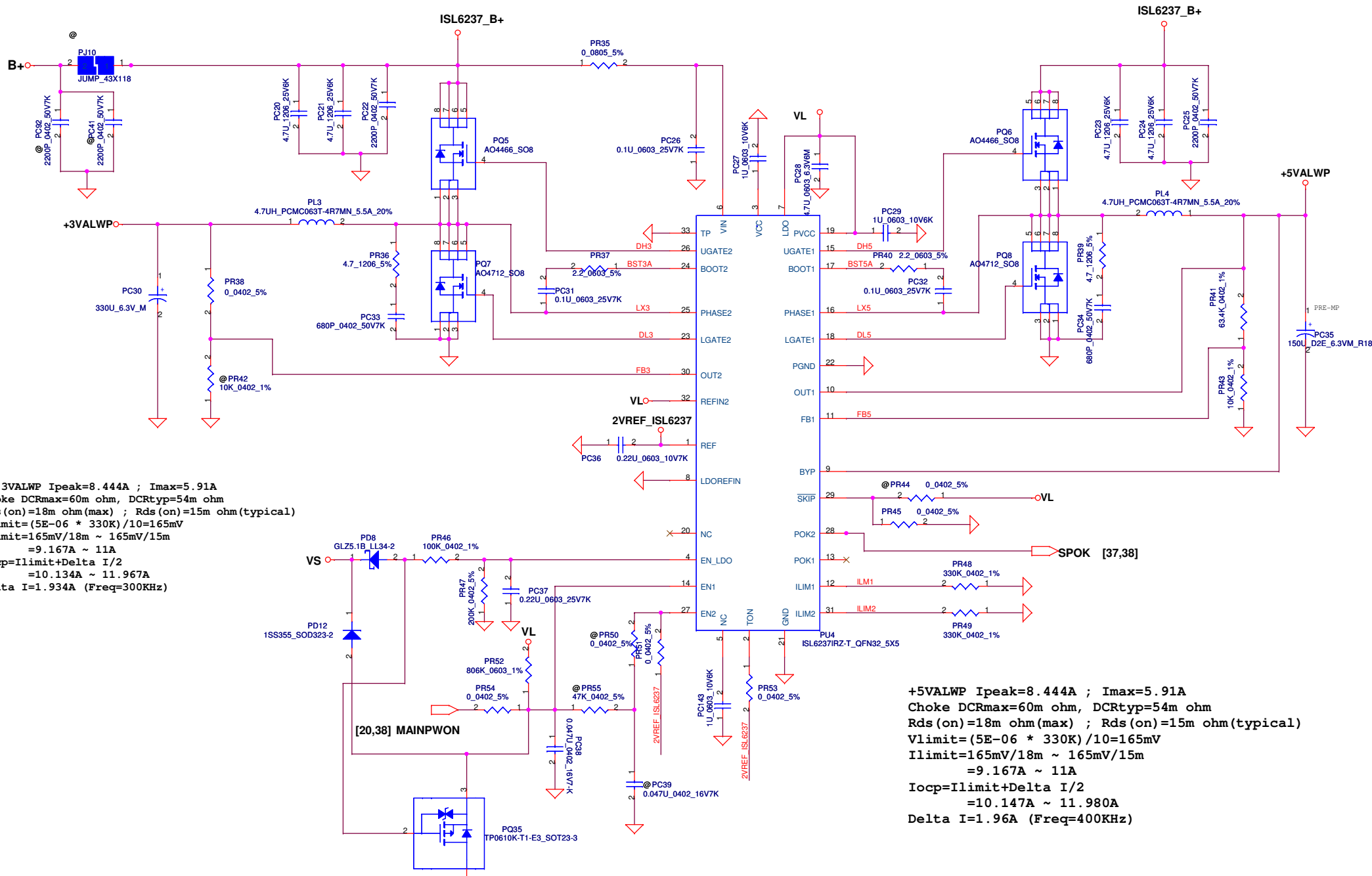
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						Size		Document Number		Rev	
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PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 47 degree C



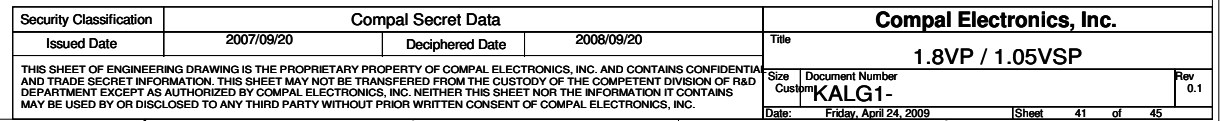
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+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
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PCB

ZZZ



LA-5272P MB Rev0: DA60000DW00

PCB 08Y LA-5271P REV1 M/B

North Bridge

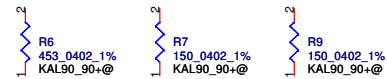
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GL40: SA00002Q8N0

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GL40@

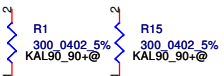
MEDIA_LED NUM_LED CAPS_LED



ON/OFF LED Risiter



Enlightener LED



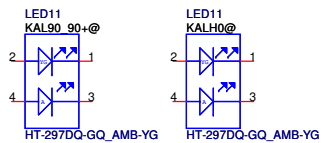
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R380 10K_0402_5% KALH0@
R399 10K_0402_5% KALH0@

PROJECT ID (KALG1_90+)

R156 10K_0402_5% KAL90_90+@
R380 10K_0402_5% KAL90_90+@
R399 10K_0402_5% KAL90_90+@

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					Option Component
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